



# Future Proofing your MicroTCA design for Serial RapidIO 2.0

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## Agenda

- MicroTCA Introduction
- sRIO 2.0 vs sRIO 1.3
- Valuable sRIO 2.0 features for a sRIO 1.3/2.0 mixed system
- Future Proofing your modular MicroTCA design for sRIO 2.0 tomorrow
- IDT- Leading the transition to sRIO 2.0

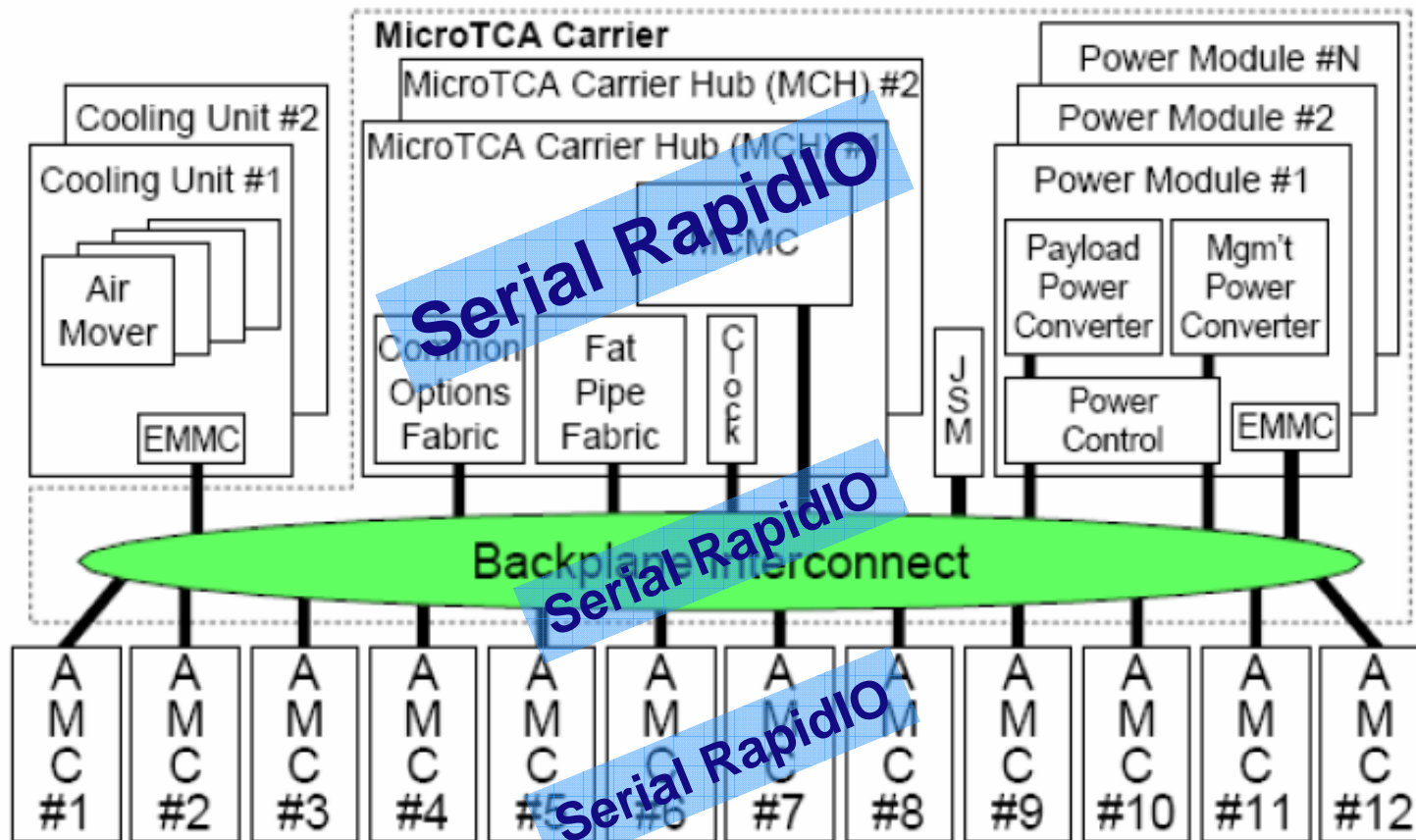


# MicroTCA Introduction

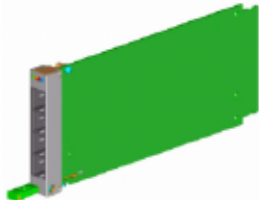
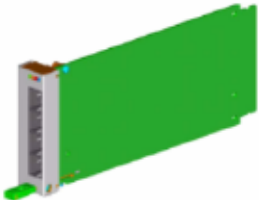
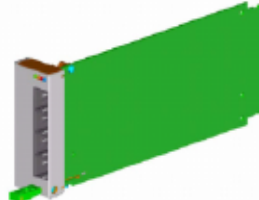
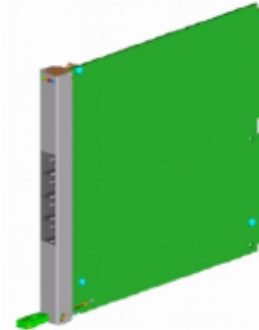
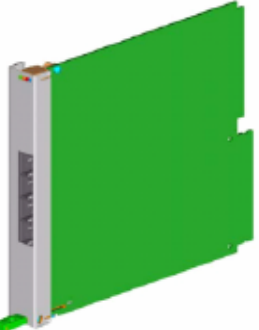
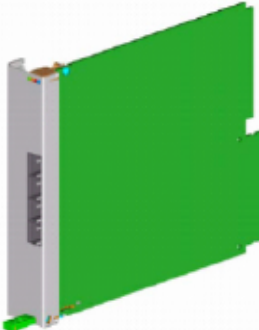
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# MicroTCA System Block Diagram

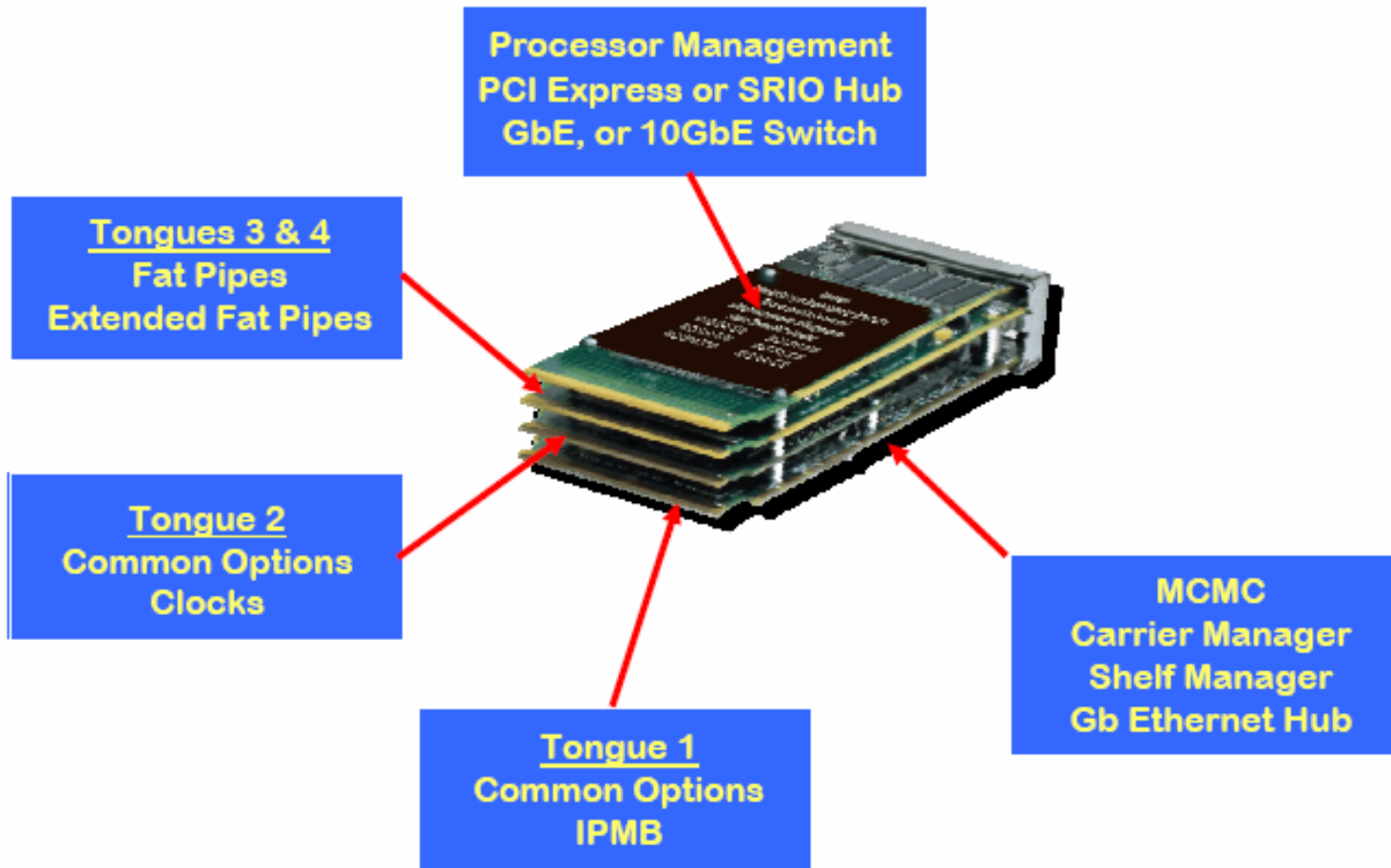


# AdvancedMCs - the primary component

	Compact-Size (3HP)	Mid-Size (4HP)	Full-Size (6HP)
Single modules	 73.8x13.88x181.5mm	 73.8x18.96x181.5mm	 73.8x28.95x181.5mm
Double modules	 148.8x13.88x181.5mm	 148.8x18.96x181.5mm	 148.8x28.95x181.5mm

AdvancedMC Module configuration examples

# MicroTCA Carrier Hub (MCH)



## MicroTCA Interconnect Protocols

- PCI Express (AMC.1)
- Ethernet (AMC.2)
- Storage Interfaces (AMC.3)
- **RapidIO (AMC.4)**
- Future subsidiary specifications of AdvancedMCs



## sRIO 2.0 vs sRIO 1.3

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# New Serial Physical Layer Feature Overview

## sRIO v1.3

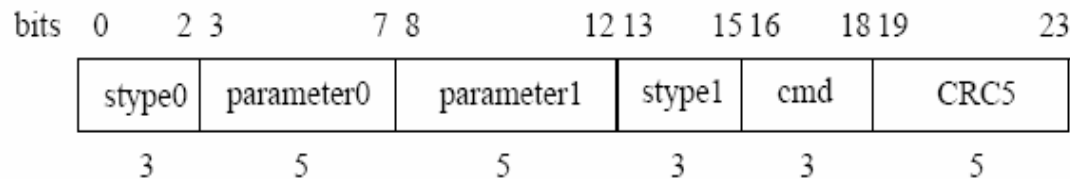
- Link width --- 1x, 4x
- Link rates --- 1.25, 2.5, 3.125 Gbaud XAUI
  - Long reach --- 50cm + 2 connectors
  - Short reach --- 20cm + 1 connectors

## sRIO v2.0

- Link width --- 1x, 2x, 4x, 8x, 16x
- Link rates ---
  - 1.25, 2.5, 3.125 Gbaud XAUI
  - 5.0, 6.25 Gbaud OIF (Optical Internetworking Forum)
    - Long reach --- 100cm + 2 connectors
    - Medium reach --- 60cm + 2 connectors
    - Short reach --- 20cm + 1 connector
    - Decision Feedback Equalization (DFE)
    - Data scrambling capability

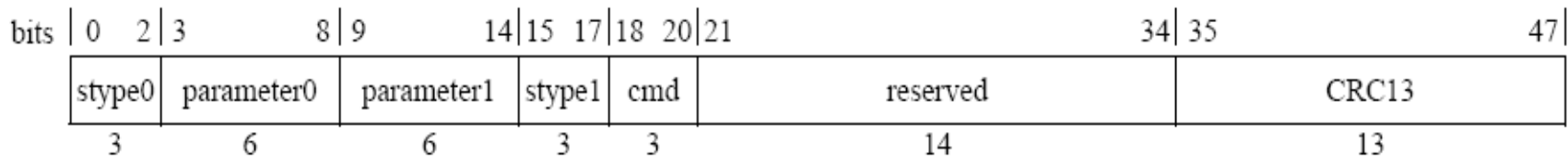
# New Control Symbol and Idle Sequence

## sRIO v1.3



- 24bits control symbol
- 5bits CRC

## sRIO v2.0



- 48bits control symbol allows for Virtual Output Queue
- 13bits CRC for better DFE based receiver
- Idle provides auto detection of lane polarity, port width/lane number, data rate
- Idle provides auto-tuning of Transmitter emphasis setting

## sRIO 2.0 Data Plane Enhancement Overview

### Addition of Virtual Channels (VC) to Serial Physical Layers

- Continuous Traffic (CT) or Reliable Traffic (RT)
- Allows reserving of bandwidth and Quality of Service (QoS) on subchannel granularity

### New Data Streaming Packet Format (Type 9)

- Add support for end-to-end flow control
- Support On/Off, Rate based, and credit based schemes

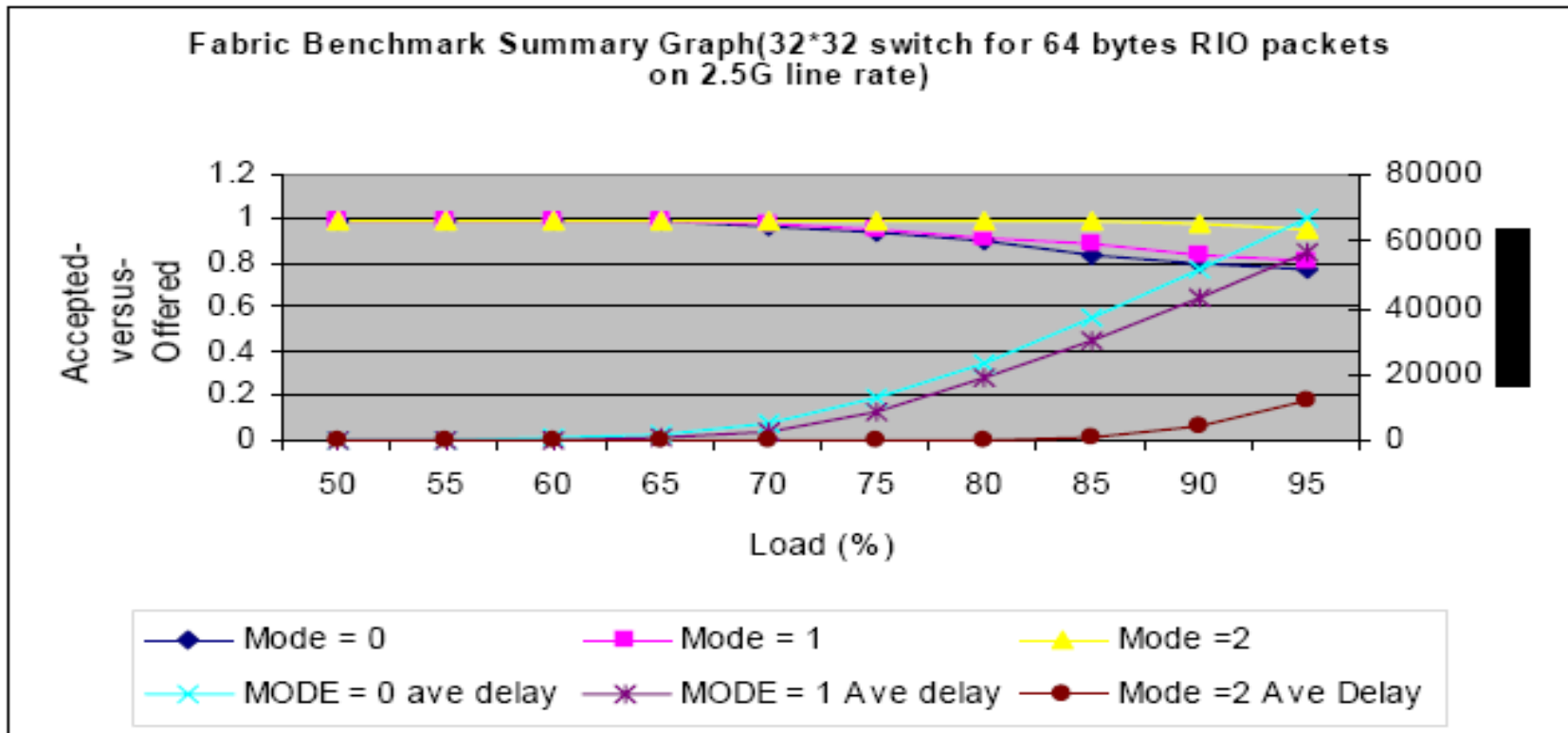
### Virtual Output Queue (VoQ) Spec

- Two-stage virtual output table support to avoid Head-of-line (HOL) blocking
- Utilize new control symbol to communicate the congestion info about downstream ports

### New Endpoint Flow Control Arbitration (Enhanced Type 7)

- Allows endpoints to manage and arbitrate for resource Segmentation and Reassembly (SAR) contents at a PDU level

# Fabric Benchmark Improvement with VC and VoQ



Mode 0 = v1.3 based traffic  
 Mode 1 = VC based  
 Mode 2 = VC + VoQ

Courtesy of Chunhua Hu. Erlang Technologies

## Summary of sRIO 2.0 Enhancements

- Higher Bandwidth, Maintaining Low Overhead
- Complete Set of Transactions
  - I/O
  - Messaging
  - Globally Shared Memory
  - Streaming Data
- Carrier Grade Data Fabric Performance
  - Deterministic Latency
  - Quality of Service
  - End to End Data Management
- Standardization of Encapsulation



# Valuable sRIO 2.0 features for a sRIO 1.3/2.0 mixed system

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## Bandwidth Scheduling Rules of sRIO 2.0

Rules	Object
Bandwidth Reservation	VC0, VC1~VC8
Strict Priority	VC0

VC0 = bandwidth reservation



- all VCs will receive their expected minimum bandwidth

VC0 = strict priority



- VC0 will get whatever bandwidth it needs
- Remaining VCs will divide up whatever portion of bandwidth remains

When a VC demands less than its guaranteed bandwidth



- Other VCs can use the available bandwidth

## Packet Transmission Modes of sRIO 2.0

### Reliable Transmission (RT)

- RT operations are like earlier versions of sRIO in that retransmitting a packet when it cannot be received makes packet transmission lossless.
- VC0 supports all defined priorities and operates exclusively in RT mode

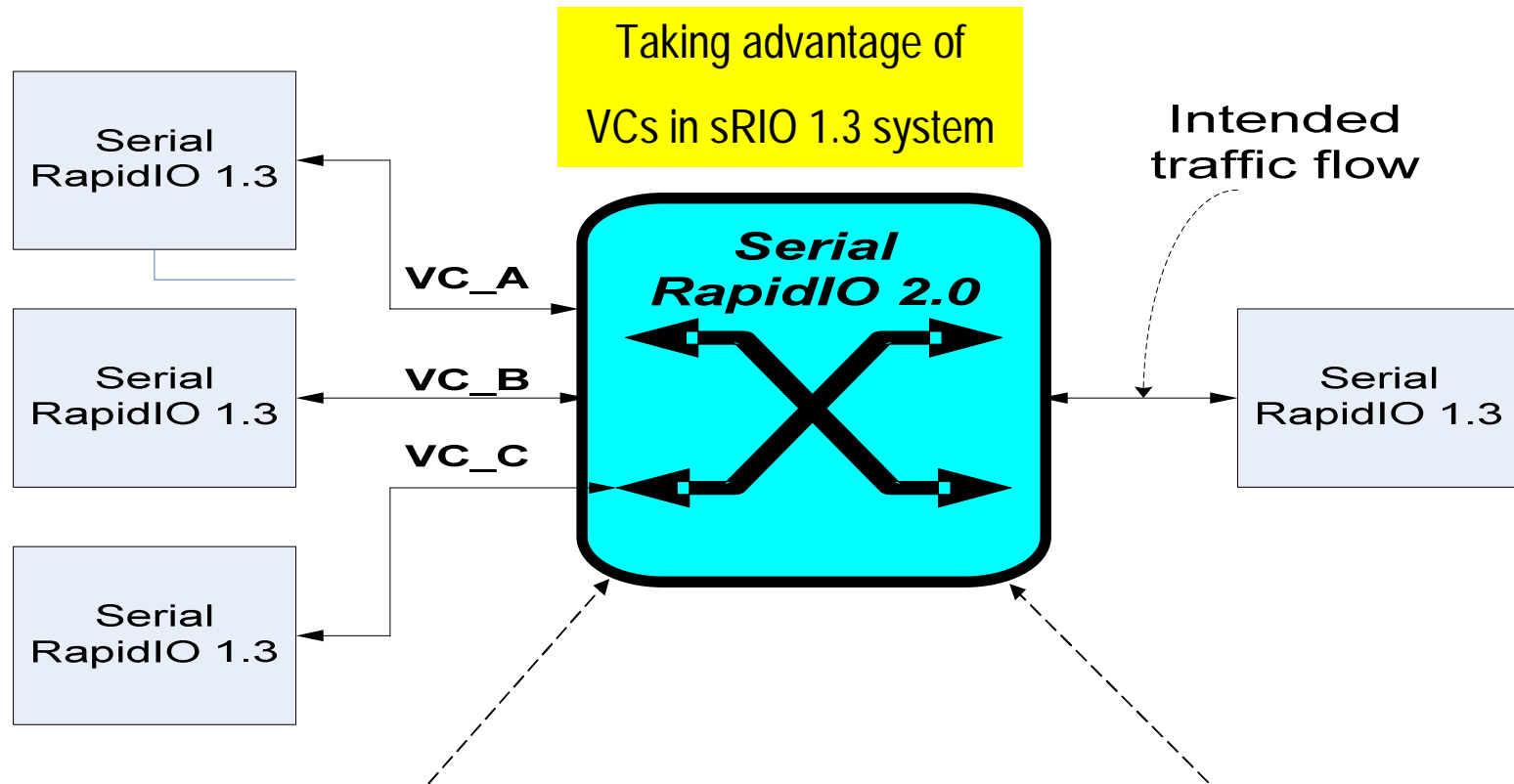
### Continuous Transmission (CT)

- CT is optimized to achieve low latency for traffic flows that can accommodate packet loss by not performing retransmissions.
- Higher VCs (1~8) can operate in CT or RT mode.

## sRIO 1.x/2.0 Mixed System Implementations

- sRIO 1.x and sRIO 2.0 product availability will overlap for an extended period of time
- Switch vendors can enable many of the sRIO 2.0 benefits independent of available sRIO 2.0 end points

# Mixed sRIO 1.3/2.0 System --- Example 1

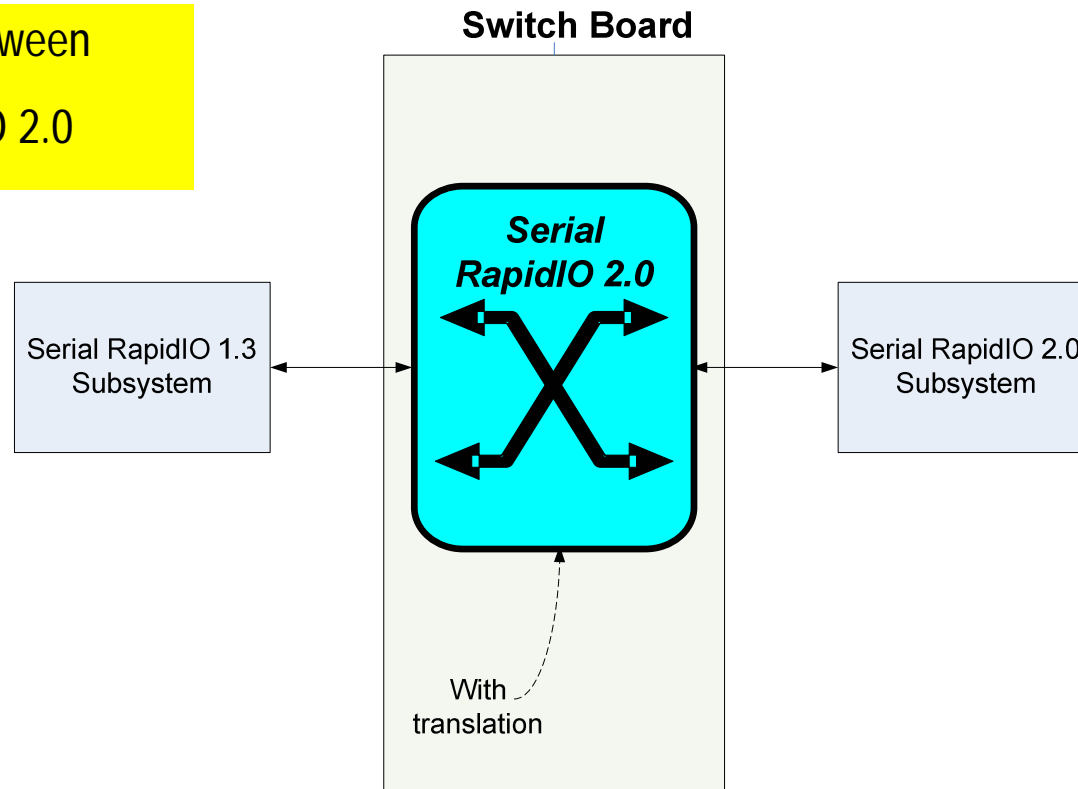


- VC mapping in the input port
  - Using a unique destination identifier to assign VCs to the incoming packet

- Pseudo CT mode in the output side
  - A new packet replaces a packet that needs to be retransmitted.

## Mixed sRIO 1.3/2.0 System --- Example 2

Communicating between  
sRIO 1.3 and sRIO 2.0



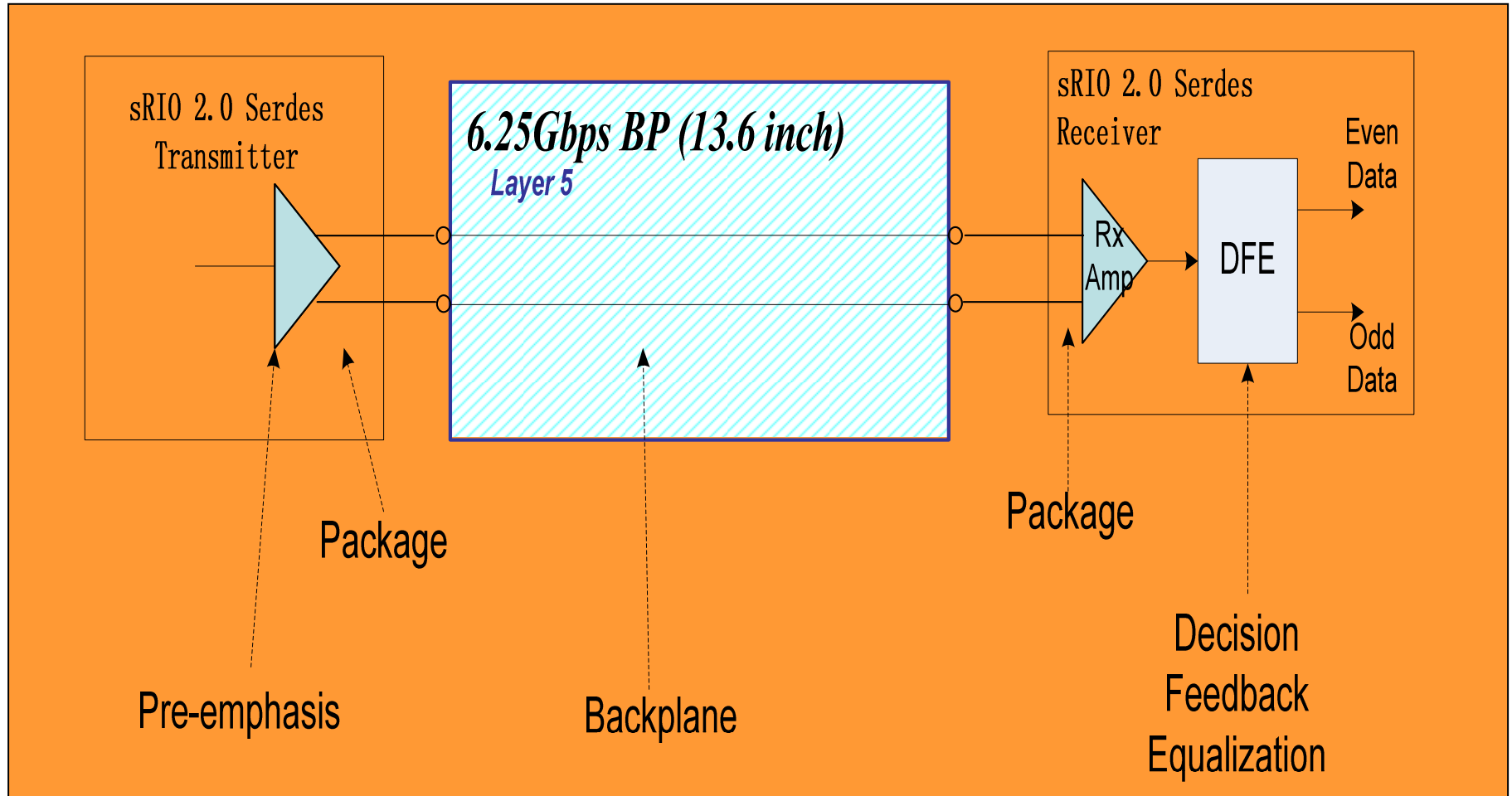
- Switch operates as a translator between sRIO 1.3 legacy traffic and sRIO 2.0 VC traffic.



# Future Proofing your modular MicroTCA design for sRIO 2.0 tomorrow:

HSPICE Simulation with 13.6 inch BP at 6.25G

# Hspice Simulation Architecture



# 22 Layer Backplane Stackup

## Backplane

Overall Thickness:		.138	+/- 10%	Er (Dielectric Constant) = 3.5		
	Dielectric	Copper	Target Impedance	Line / Space	Calc	
1	----- .0053	Signal 1.5 oz	50 to 75 ohms	.007	57.2	
2	----- .006	Plane .5 oz			50.1	
3	----- .0062	Signal .5 oz	{ 50 ohms +/- 10% 100 Differential +/- 10%	.00625 / .020	99.91	
4	----- .006	Plane .5 oz			50.1	
5	----- .0062	Signal .5 oz	{ 50 ohms +/- 10% 100 Differential +/- 10%	.00625 / .020	99.91	
6	----- .006	Plane .5 oz			50.1	
7	----- .0062	Signal .5 oz	{ 50 ohms +/- 10% 100 Differential +/- 10%	.00625 / .020	99.91	
8	----- .006	Plane .5 oz			50.1	
9	----- .0062	Signal .5 oz	{ 50 ohms +/- 10% 100 Differential +/- 10%	.00625 / .020	99.91	
10	----- .006	Plane .5 oz			50.1	
11	----- .0062	Signal .5 oz	{ 50 ohms +/- 10% 100 Differential +/- 10%	.00625 / .020	99.91	
12	----- .006	Plane .5 oz			50.1	
13	----- .0062	Signal .5 oz	{ 50 ohms +/- 10% 100 Differential +/- 10%	.00625 / .020	99.91	
14	----- .006	Plane .5 oz			50.1	
15	----- .0062	Signal .5 oz	{ 50 ohms +/- 10% 100 Differential +/- 10%	.00625 / .020	99.91	
16	----- .006	Plane .5 oz			50.1	
17	----- .0062	Signal .5 oz	{ 50 ohms +/- 10% 100 Differential +/- 10%	.00625 / .020	99.91	
18	----- .006	Plane .5 oz			50.1	
19	----- .0062	Signal .5 oz	{ 50 ohms +/- 10% 100 Differential +/- 10%	.00625 / .020	99.91	
20	----- .002	Ground .5 oz				
21	----- .003	Power .5 oz				
22	-----	Ground 1.5 oz				
		.1383	Final Thickness (After Plating)			

New Layers {

- 1) Approval of this stack-up supersedes fabrication drawing requirements
- 2) Some laminates require special order and additional lead time.

SI

$$\epsilon_R = 3.5$$

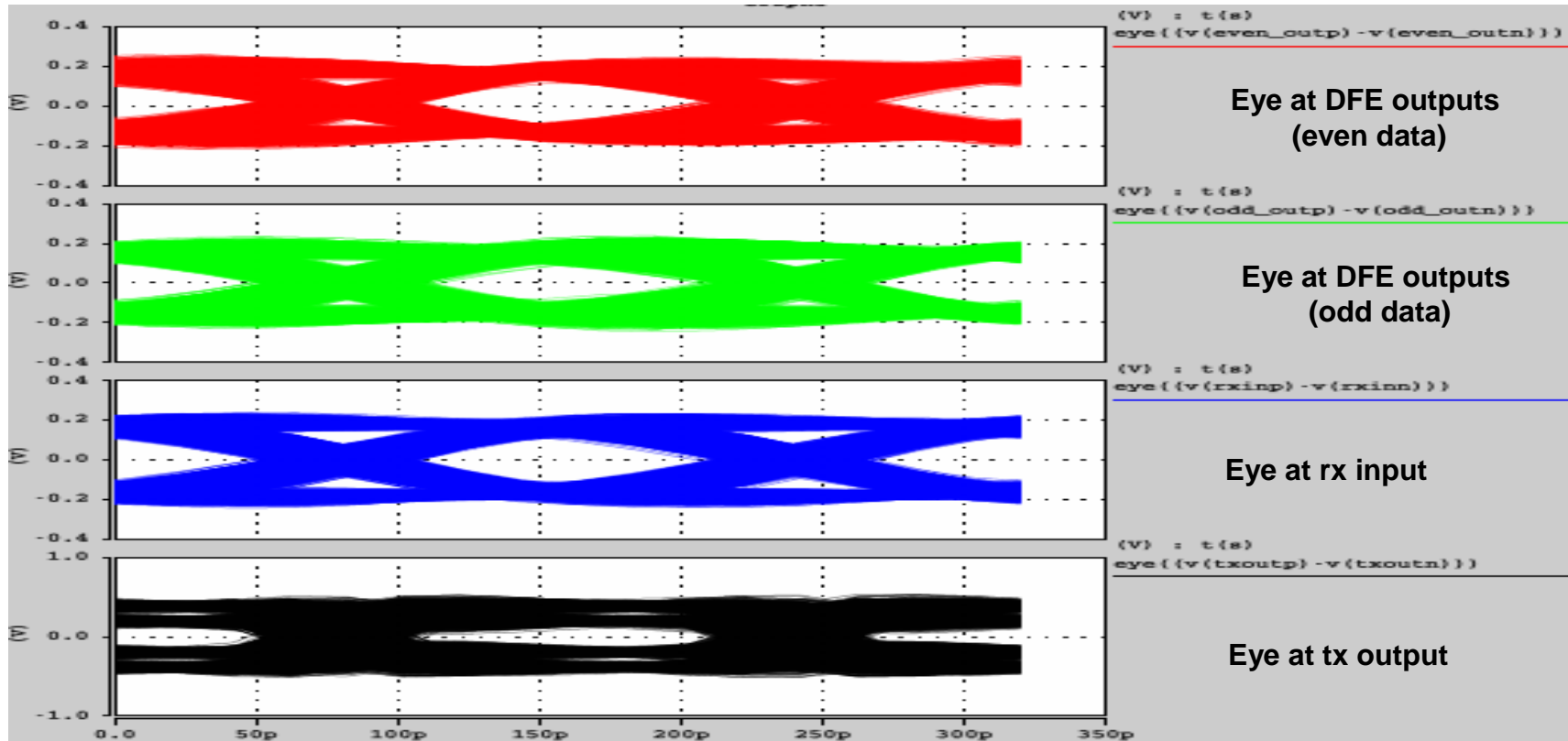
$$\text{Tan } \delta = 0.008 @ 2.5 \text{ GHz}$$

### Electrical Properties

Dielectric Constant (50% resin content)		
@ 1 GHz (RF Impedance)	3.7	3.4
@ 2.5 GHz (Split Post Cavity)	3.7	3.2
@ 10 GHz (Stripline)	3.6	3.2
@ 10 GHz (Split Post Cavity)	3.7	3.3
Dissipation Factor (50% resin content)		
@ 2.5 GHz (Split Post Cavity)	0.009	0.008
@ 10 GHz (Stripline)	0.009	0.008
@ 10 GHz (Split Post Cavity)	0.008	0.007

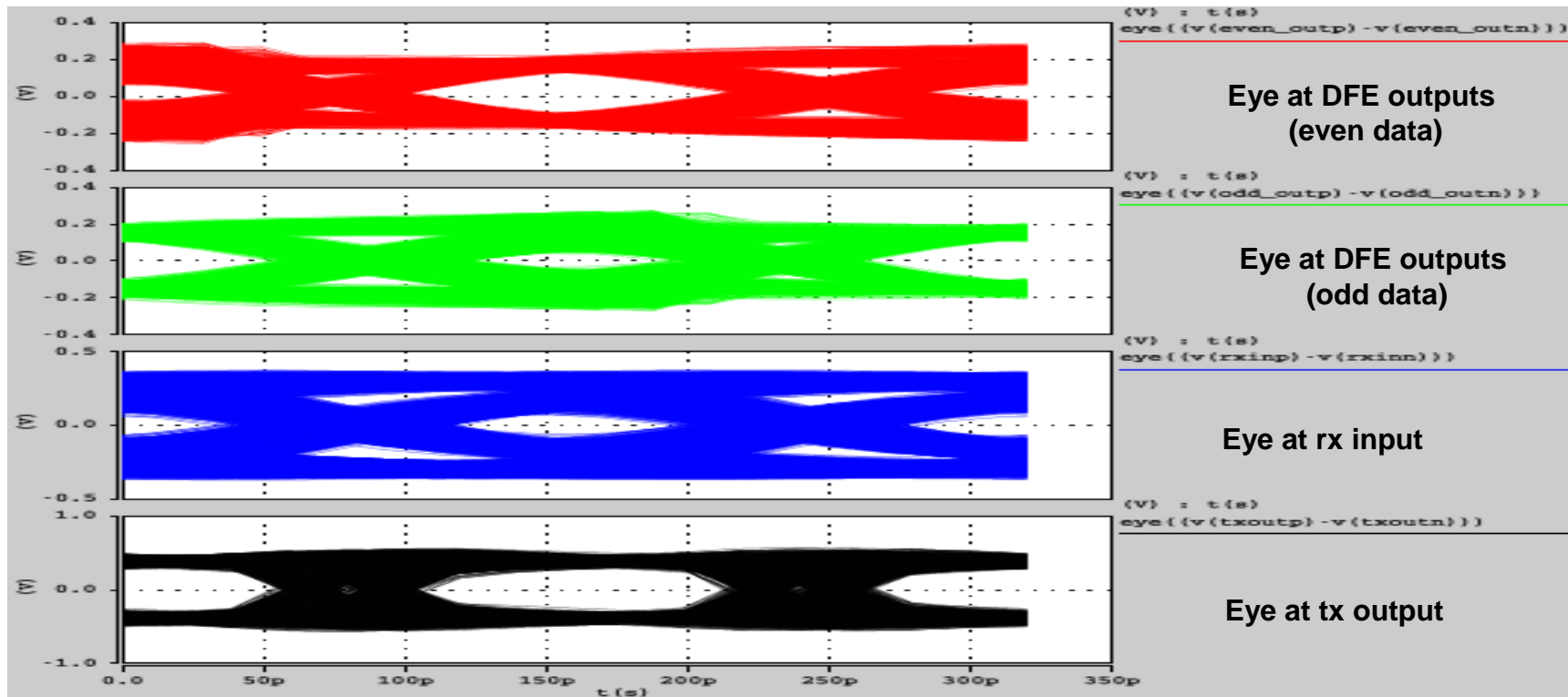
Layer 5 Escape: 6.25/20/6.25 Pair

## 6.25G eye Pre-emphasis Only, No DFE, No Package model



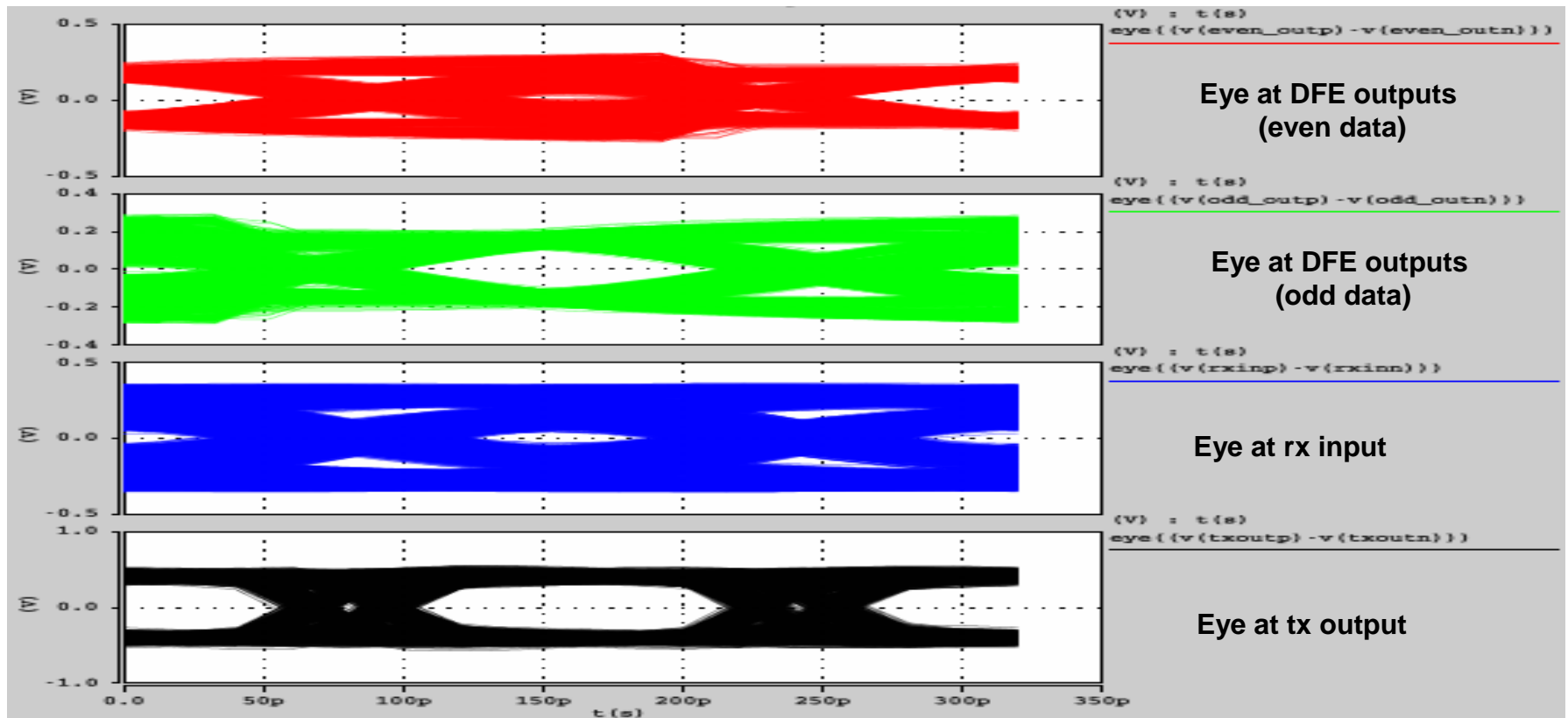
- Tx pre-emphasis is able to open the eye at the input of Rx

## 6.25G eye No Pre-emphasis, DFE On, No Package model



- The eye at the Rx input got much smaller.
- However the DFE is able to open it up.

## 6.25G eye No Pre-emphasis, DFE On, Plus Package model



- The eye at Rx input is further reduced
- The DFE is able to open the eye nicely.

## Hardware Proposal for MicroTCA system that is upgradeable to sRIO 2.0

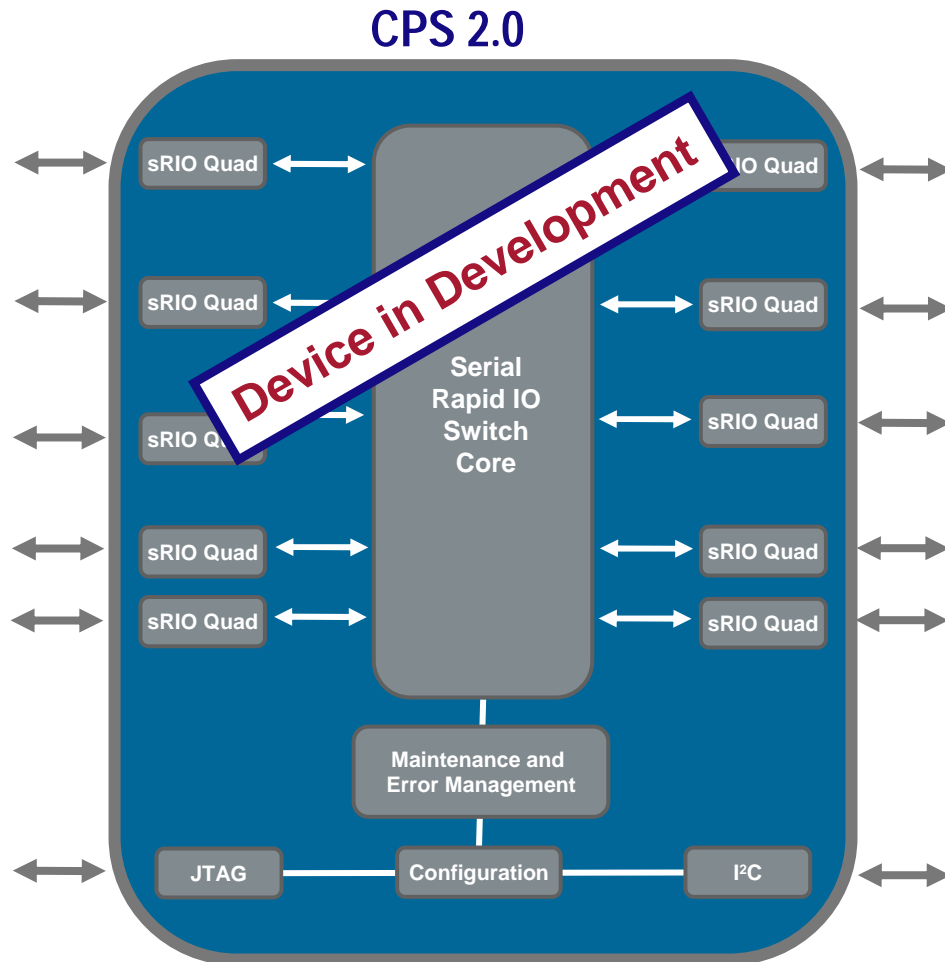
- **Design will be MicroTCA based**
  - Cost-effective modular standard
  - Leverages existing infrastructure and COTS boards
  - sRIO 1.3 AMCs & MCHs are readily available now
- **MicroTCA backplane and cards designed for sRIO 2.0**
  - Can be designed today for a 12-slot backplane in FR4 @ 6.25G
  - Is a future-proof design for evolution from sRIO 1.3 to mixed sRIO to full sRIO 2.0
  - sRIO 2.0 components will be available ~2010



# **IDT - Leading The Transition to sRIO 2.0**

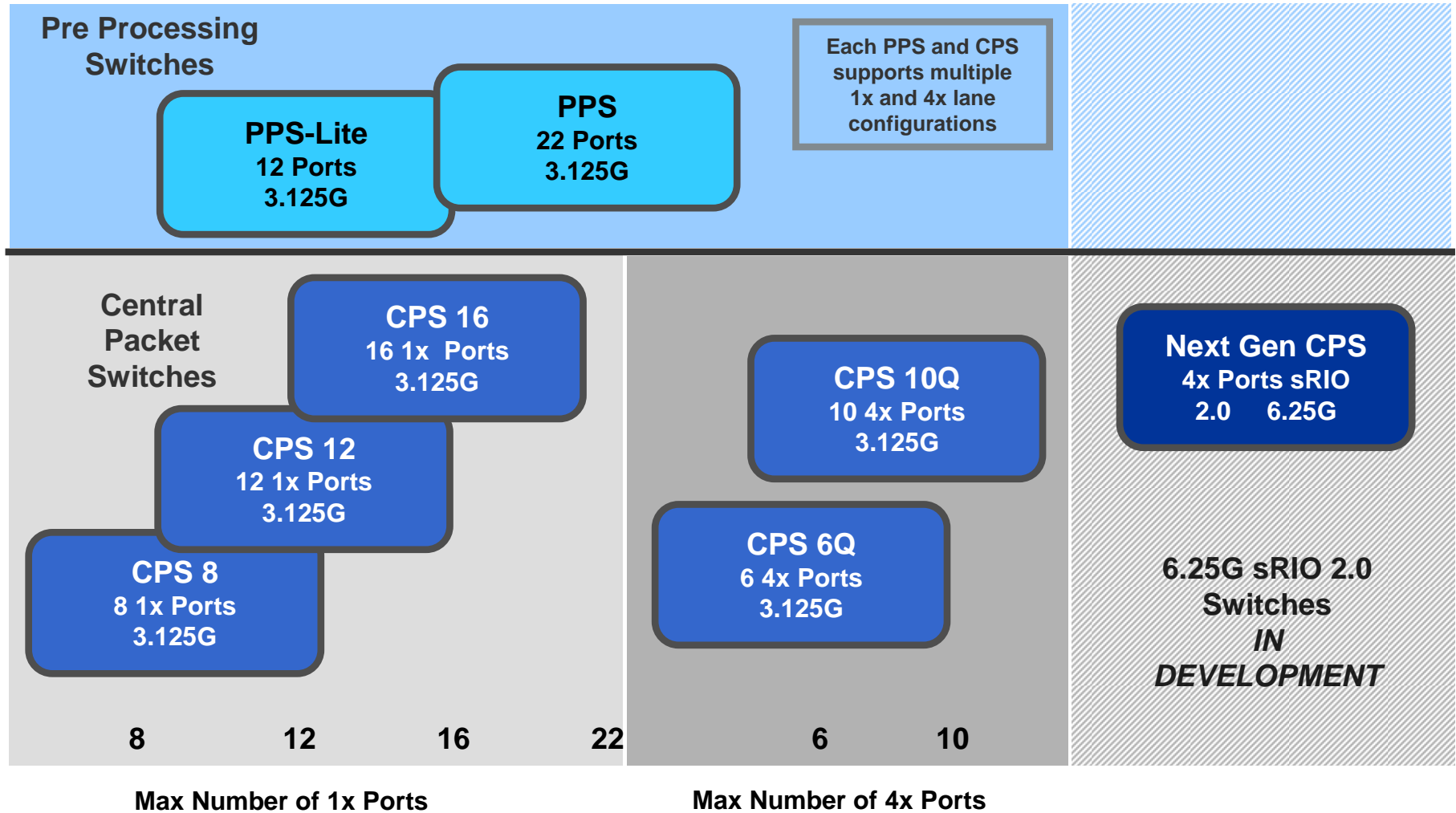
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## 3rd Generation CPS: Supporting 6.25G sRIO 2.0



- **Lanes**
  - All lanes will support 1.25, 2.5, 3.125, 5, and 6.25 Gbps
  - Backwards compatible with sRIO 1.3
  
- **Switch core performance**
  - Highest throughput
  - Lowest latency
  
- **Contact IDT for availability**

# IDT - Expanding sRIO Switching Solutions





# IDT sRIO Switch Comparison Matrix

Device	PPS 70K2000	PPS Gen 2 80KSW0001	CPS-16 80KSW0002	CPS-12 80KSW0004	CPS-8 80KSW0003	CPS-10Q 80KSW0005	CPS-6Q 80KSW0006
<b>Ports</b>	22 1x ports 10 4x ports Mix of both	12 1x ports 3 4x ports Mix of both	16 1x ports 4 4x ports Mix of both	12 1x ports 3 4x ports Mix of both	8 1x ports 2 4x ports Mix of both	10 4x ports 16 1x ports Mix of both	6 4x ports 16 1x ports Mix of both
<b>Package</b>	27 x 27mm, 676 pin	19 x 19mm, 324 pin 27 x 27mm, 676 pin	19 x 19mm, 324 pin	19 x 19mm, 324 pin	19 x 19mm, 324 pin	27 x 27mm, 676 pin	27 x 27mm, 676 pin
<b>Features</b>	Store and Forward  Multicast Non-blocking within each sRIO priority 10 Pre-Processing Scenarios Error Handling  SerDes BIST	Store and Forward  Multicast Non-blocking within each sRIO priority 4 Pre-Processing Scenarios Error Handling Packet Trace / Mirror Packet Filter / Kill SerDes BIST	Store and Forward Cut Through Multicast Non-blocking within each sRIO priority  Error Handling Packet Trace / Mirror Packet Filter / Kill SerDes BIST	Store and Forward Cut Through Multicast Non-blocking within each sRIO priority  Error Handling Packet Trace / Mirror Packet Filter / Kill SerDes BIST	Store and Forward Cut Through Multicast Non-blocking within each sRIO priority  Error Handling Packet Trace / Mirror Packet Filter / Kill SerDes BIST	Store and Forward Cut Through Multicast Non-blocking within each sRIO priority  Error Handling Packet Trace / Mirror Packet Filter / Kill SerDes BIST	Store and Forward Cut Through Multicast Non-blocking within each sRIO priority  Error Handling Packet Trace / Mirror Packet Filter / Kill SerDes BIST
<b>Aggregate Peak Throughput</b>	100G PPScs 10G Switch 100G Combined (port limited)	30G PPScs 30G Switch 30G Combined (port limited)	40G	30G	20G	100G	60G
<b>Status</b>	<b>Production</b>	<b>Production</b>	<b>Production</b>	<b>Production</b>	<b>Production</b>	<b>Sampling NOW</b>	<b>Sampling NOW</b>



# Functional InterConnect and Serial Buffer Portfolio

Device	FIC 80HFC1000	FIC 80HFC1001	FIC 80KFC1002	Serial Buffer 80KSB201
<b>Ports</b>	3 CPRI 1 sRIO (1x or 4x)	3 CPRI 2 TDM (16 bit ports)	1 sRIO (1x or 4x) 1 Parallel (QDRII Burst of 2)	2 sRIO (1x or 4x) 1 Parallel (QDRII Burst of 2)
<b>Package</b>	19 x 19mm, 324 pin	19 x 19mm, 324 pin	23 x 23mm, 484 pin	23 x 23mm, 484 pin
<b>Features</b>	<p>CPRI v2.1 compliant</p> <p>CPRI Master mode</p> <p>sRIO 1.3 compliant</p> <p>Programmable mapping</p> <p>Supports sRIO maintenance operations</p>	<p>CPRI v2.1 compliant</p> <p>Each CPRI port configurable as Master or Slave to support Chain configurations</p> <p>TDM interfaces support two channel configurations</p> <p>TDM control pins provided for seamless connection to popular ADC/ DAC / DUC/ DDC devices</p> <p>Multiplexing mode options</p>	<p>sRIO 1.3 compliant</p> <p>Parallel port for external processor, FPGA, or memory</p> <p>10Gbps throughput</p> <p>Status flags and Water marks</p>	<p>18 Mbits on-chip memory, expandable to 90 Mbits with external memory</p> <p>Configurable queue sizes</p> <p>Status flags and Water marks</p> <p>sRIO 1.3 compliant</p> <p>10Gbps throughput</p>
<b>Performance</b>	<p>CPRI: 614.4 / 1228.8 / 2457.6 Mbaud</p> <p>sRIO: 1.25 / 2.5 / 3.125 Gbaud</p>	<p>CPRI: 614.4 / 1228.8 / 2457.6 Mbaud</p> <p>TDM: up to 150 MHz per port</p>	<p>sRIO: 1.25 / 2.5 / 3.125 Gbaud</p> <p>Parallel: 64-bits up to 200MHz</p>	<p>sRIO Ports : 1.25 / 2.5 / 3.125 Gbaud</p> <p>Parallel: 64-bits up to 200MHz</p>

## IDT is Committed to Serial RapidIO Solutions Now and in the Future

- Widest sRIO product portfolio through successful new product introductions
  - PPS, PPS Gen 2, CPS 16/12/8, CPS-10Q/6Q, Serial Buffer, CPRI FICs, Parallel FIC
- Excellent product execution + Outstanding customer support = clear market leadership in sRIO
  - Tremendous momentum on PPS/CPS design wins in past year
- Use of experienced, proven in-house resources to create next generation solutions for wireless infrastructure
  - Higher bandwidth switch core with sRIO 2.0
  - Strong partner relationships allow us to coordinate with and complement future DSPs
- Longevity as a solid, reputable supplier



# Questions?

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# Future Proofing your MicroTCA design for Serial RapidIO 2.0

## Thank you