

Design implementation of RapidIO in Wireless Infrastructure Subsystem

Texas Instruments

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Agenda

- Wireless Standards
- Past & present DSP interconnects
- Serial RapidIO™ Integrates with DSP
- DSP Interconnection options
- Base band subsystem Configurations
- Summary

Requirements: Single Platform – Multiple Standards, Form-Factors



TD-SCDMA



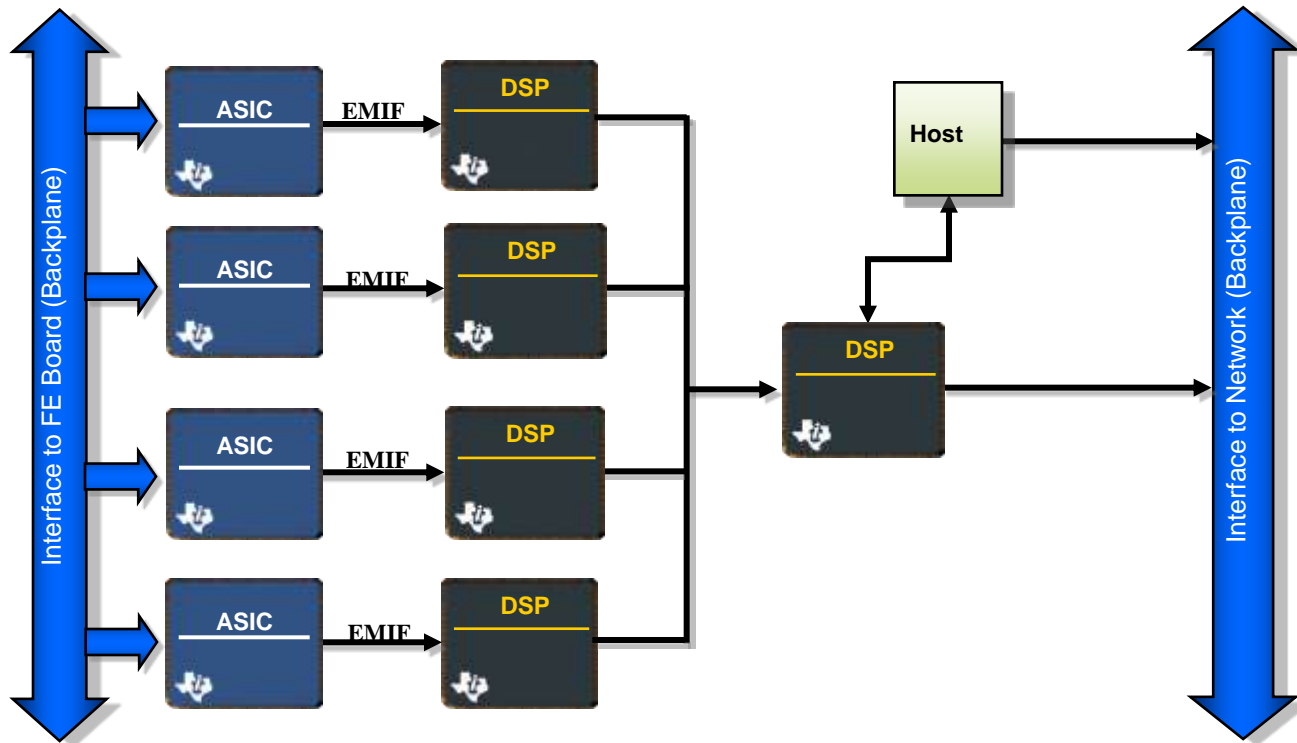
GSM-EDGE, WCDMA-HSPA, WiMAX and
LTE Software Libraries



Customers can develop high-performance products for multiple applications on a single platform using TI software libraries thus protecting their technology investment



Past 3G Baseband Uplink Simplified Architecture



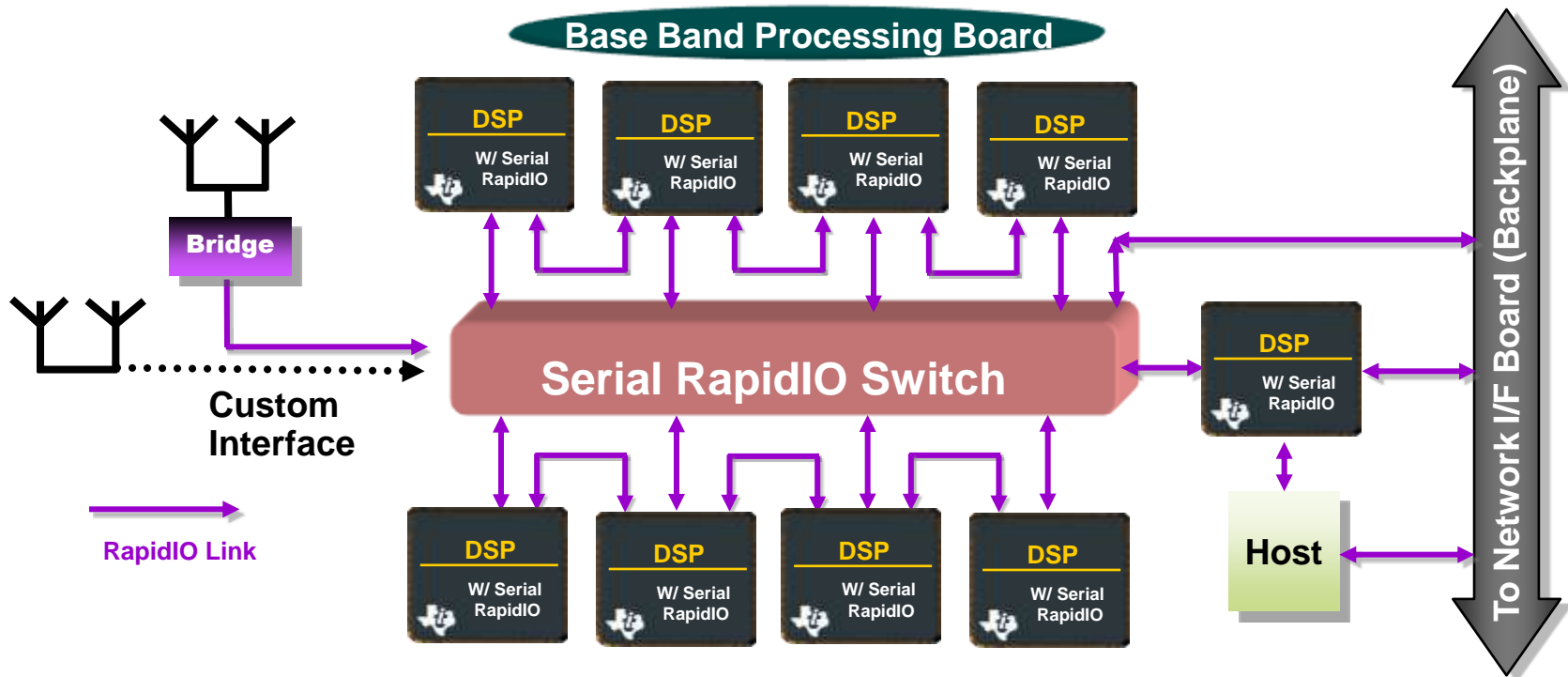
ANTENNA DATA

- Typically Performed by ASIC/FPGA
- 24-48 Antenna Streams per base station
- ~123 Mbps per antenna stream
- = 3-6 Gbps of antenna data

USER DATA

- Typically done on DSP
- 10-20Mbps per user channel
- Brought in by shared EMIF
- I/O restrictions limit channel density

Potential 3G Base Band Uplink Evolution



ANTENNA DATA

- ◆ Same data rate as before
 - ◆ 24-48 antenna streams per base station
 - ◆ ~123 Mbps per antenna stream
 - ◆ = 3-6 Gbps of antenna data

USER DATA

- Better core and I/O allow for increased density
- ~10-20 Mbps per user channel
- RIO also enables flexible architectures for soft solutions

Serial RapidIO[®] Overview

Serial RapidIO is a high-performance, packet-switched, interconnect technology that addresses the embedded industry's need for:

RELIABILITY

INCREASED BANDWIDTH

FASTER BUS SPEEDS

Serial RapidIO allows chip-to-chip and board-to-board communications at performance levels scaling to ten Gbps and beyond



- C64x+™ Serial RapidIO Support – IEEE 1149.6 Compliant
 - 1.25, 2.5, 3.125 GBaud/sec per link (1.0, 2.0 and 2.5 GBits/sec w/ 8B/10B encoding)
 - Up to four 1x links (each 1x link is bidirectional) – **OR** –
 - One 4x link (bi-directional pipe), which provides up to 12.5 GBaud/sec raw
 - Up to 10Gbps for 4x link with 8B/10B encoding
 - Resulting data range 4 - 10 Gbits / sec in each direction (up to 1.25 GBytes/sec)
 - Supports DSP to DSP on the same board, DSP to Switch, etc.
- Layered architecture to minimize impact on software
- Non-proprietary multi-vendor support
- Flexible and scalable
- Reduces chip count, board area and system cost

Serial RapidIO™ Integration Advantages

•Data Flow

- “Push” or “Pull” data flow supported
- Support for Message Passing and Direct I/O
- Prioritization of data for efficient handling by DMA system

•Control

- Configurable CPU Interrupt control, with rate-limiting
- Support for Error Management
- Support for Congestion Control

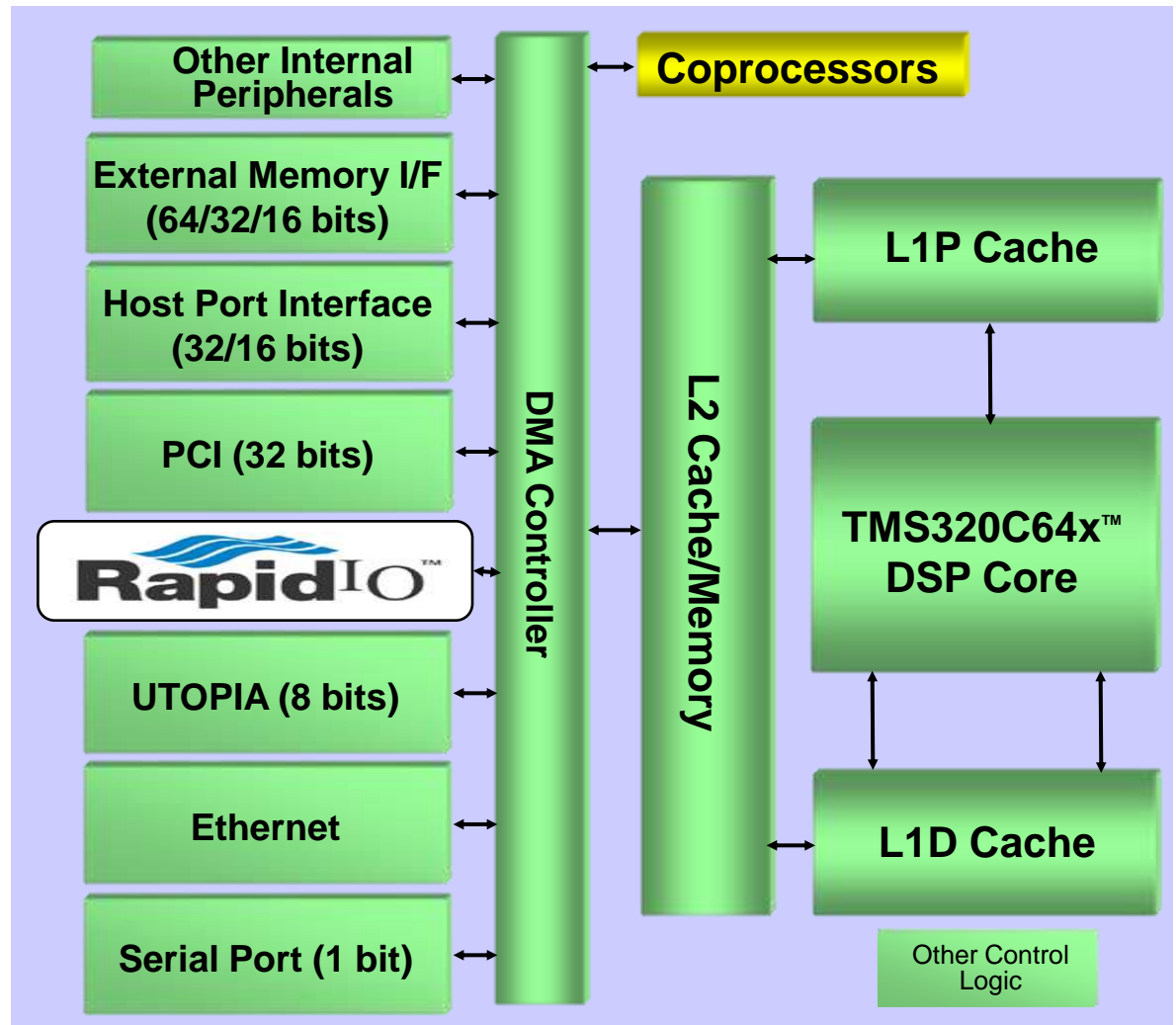
•Software Support

- Low Software overhead requires minimal CPU time
- Low level configuration and functional support
- Highly abstracted message-passing API

Serial RapidIO™ Integrates with DSP

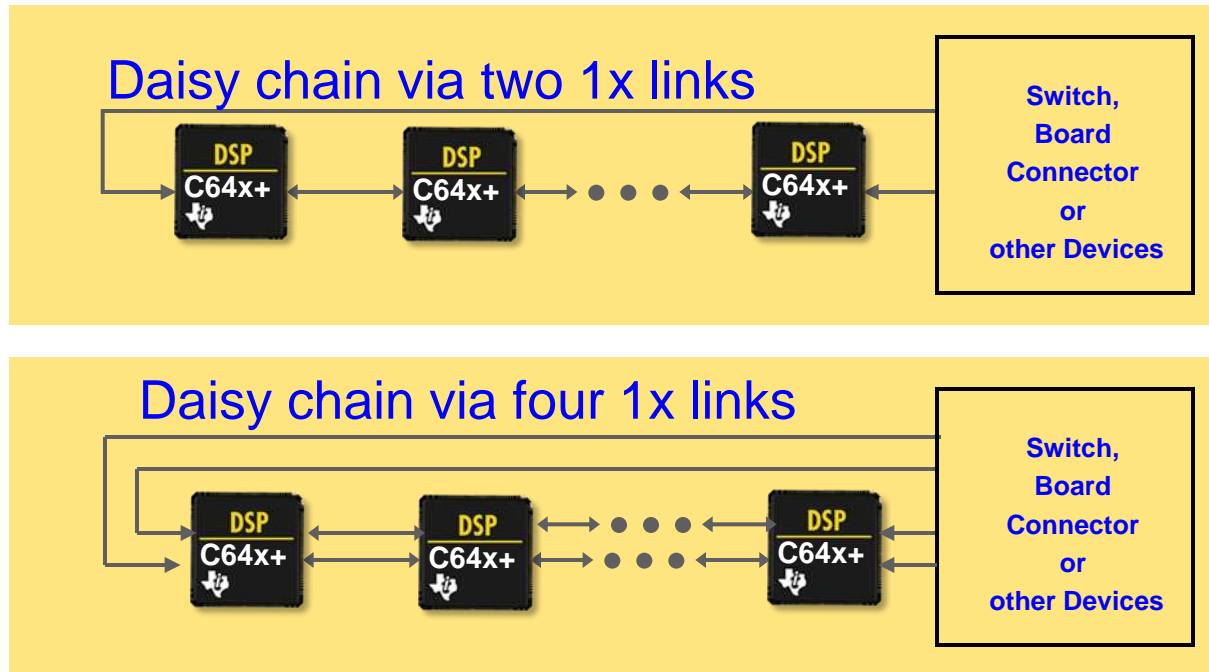
Key Features

- Interfaces directly to DMA Engine
- Uses transaction proxy registers for low control overhead
- Can queue multiple transactions
- Capable of accessing entire DSP address space
- Can Boot DSP with or without auxiliary EEPROM



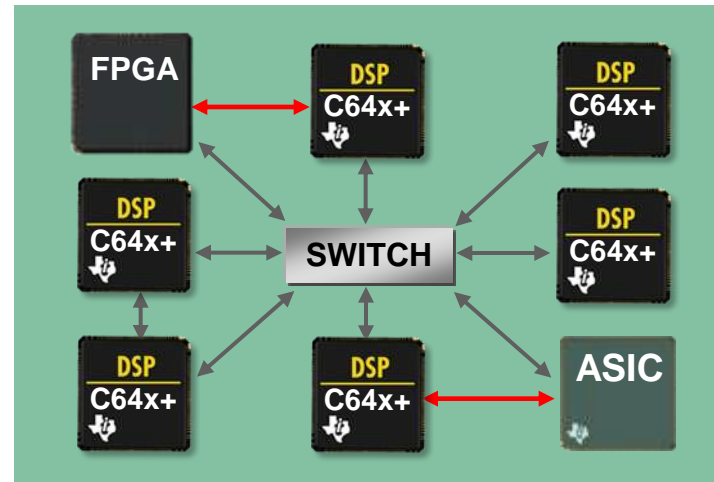
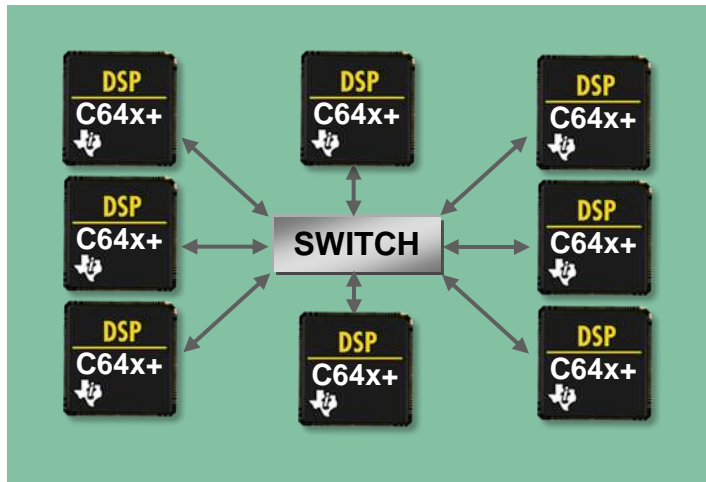
RapidIO Connectivity Options

RapidIO Daisy Chain



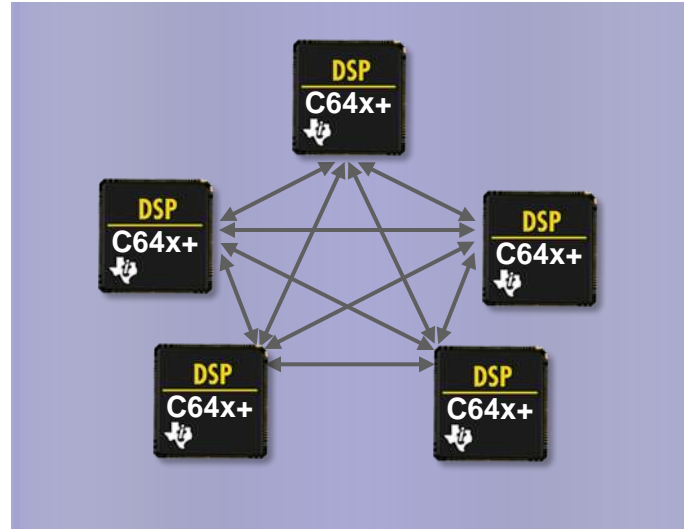
- Connect 2 / 4 lanes from DSP to DSP or other devices with RapidIO Interface
- Ideal for applications where multiple hops is acceptable
- Can be used without switch

RapidIO Switch Interconnect



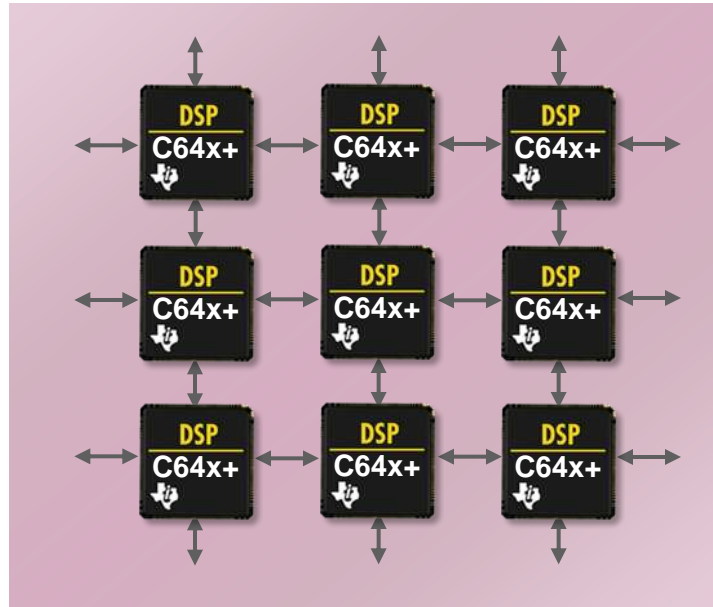
- Connect multiple DSPs to RapidIO switch via 1x or 4x lanes for DSP Farm
- For specific function where latency is critical or continuous data exchange is expected, local interconnection can be established
- Ideal where high bandwidth is needed to each device (vs daisy chain)

Direct Interconnected RapidIO



- Five DSPs are completely connected
- Provides direct connection from 1 device to any other device
- Reduces latency but limited to 1x lane bandwidth to each device

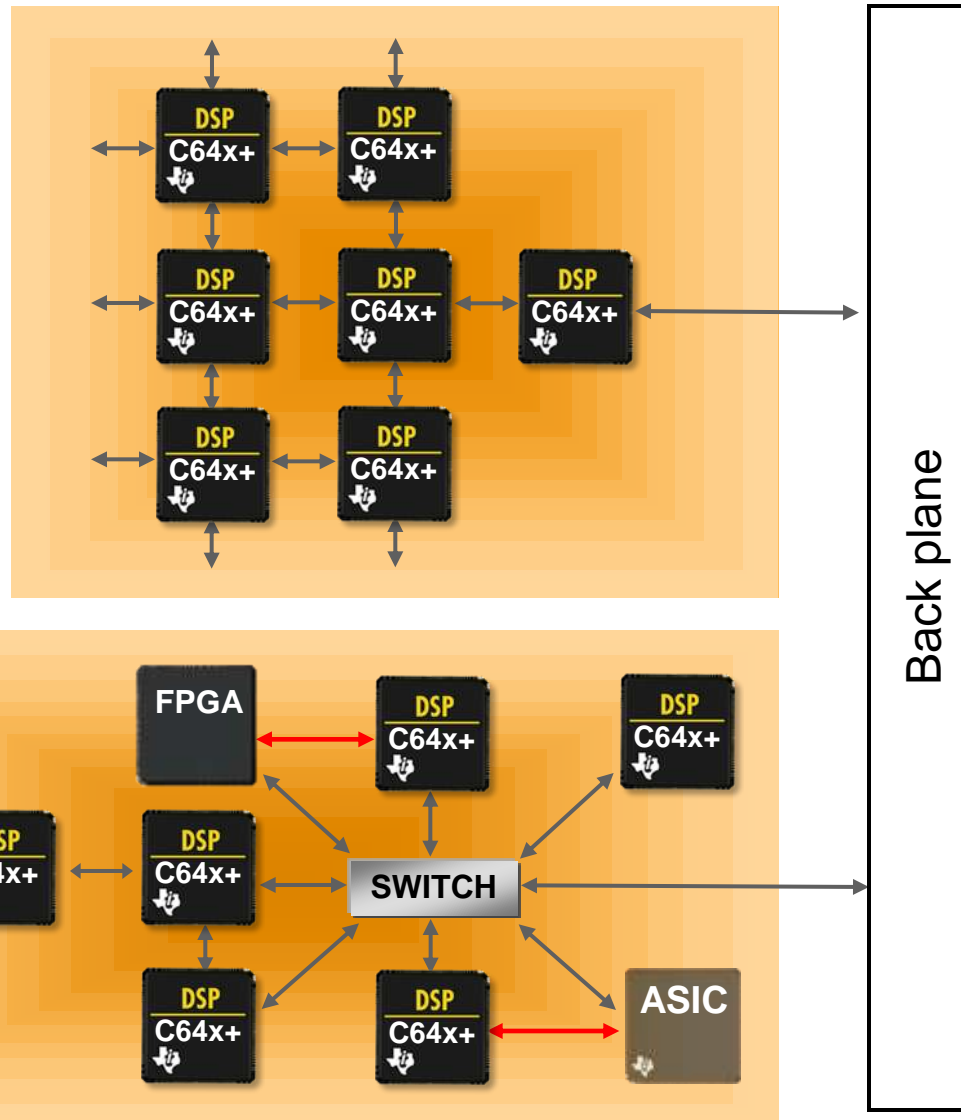
Mesh Network Configuration



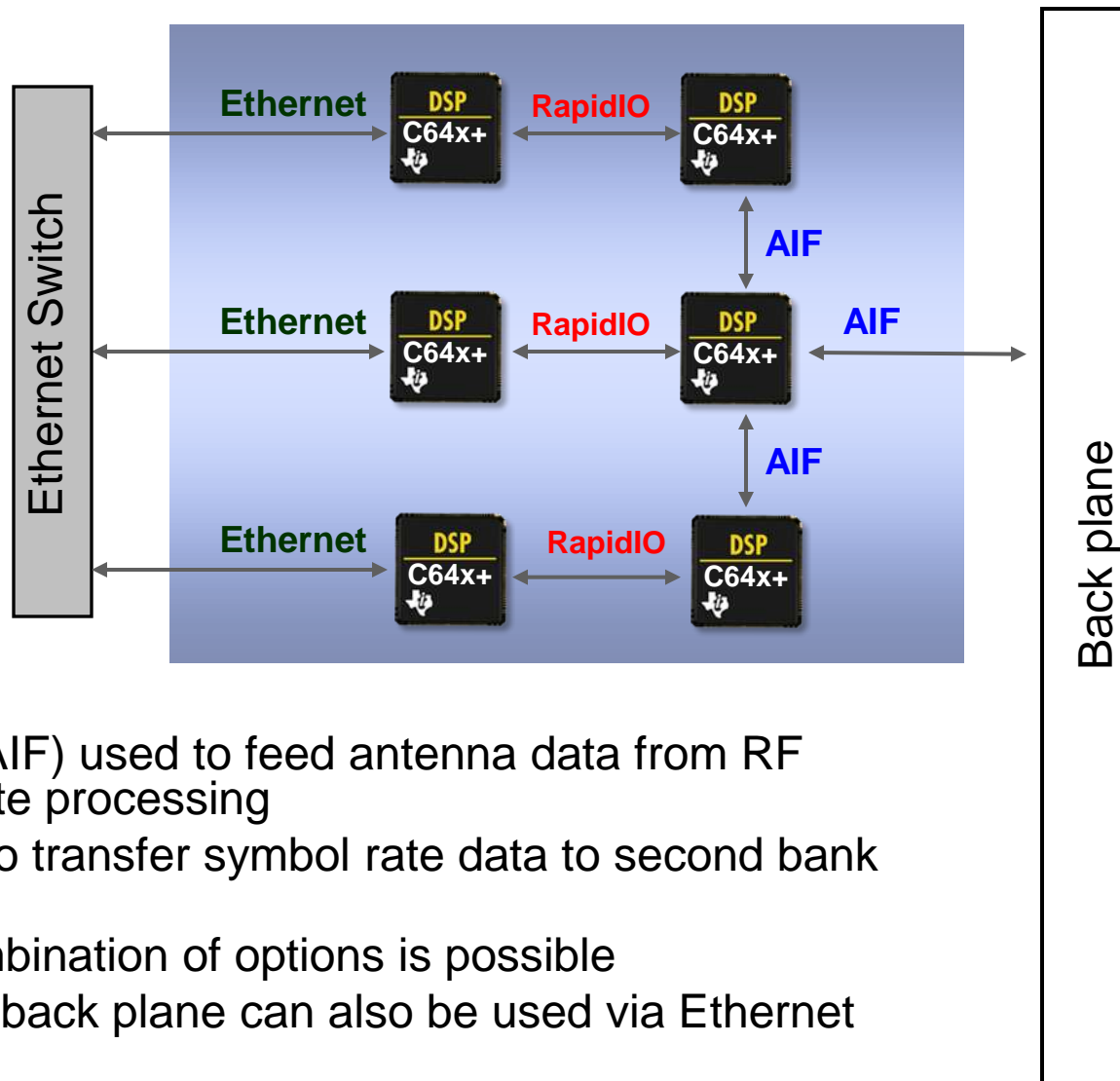
- Mesh configuration with four 1x lanes
- Can be used in different mesh configurations depending upon number of RapidIO lanes available

Combination Interconnect

- Use of any combination of options is possible
- Connectivity via RapidIO to back plane can also be used

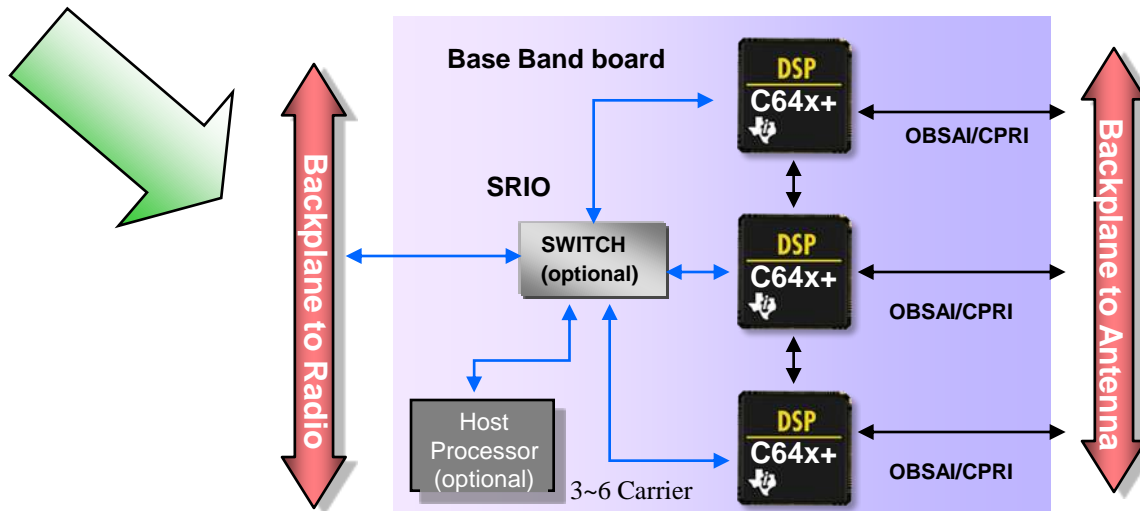
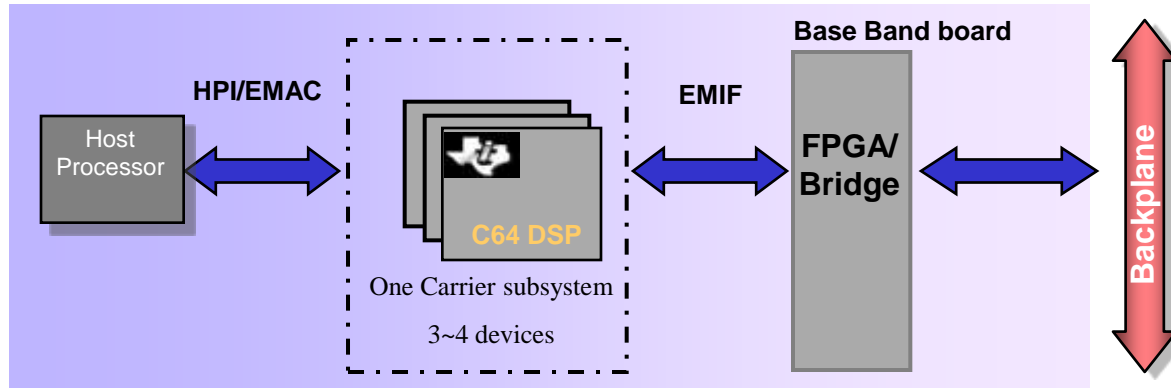


Combination Interconnect



- OBSAI/CPRI (AIF) used to feed antenna data from RF card for chip rate processing
- RapidIO used to transfer symbol rate data to second bank of DSP
- Use of any combination of options is possible
- Connectivity to back plane can also be used via Ethernet switch

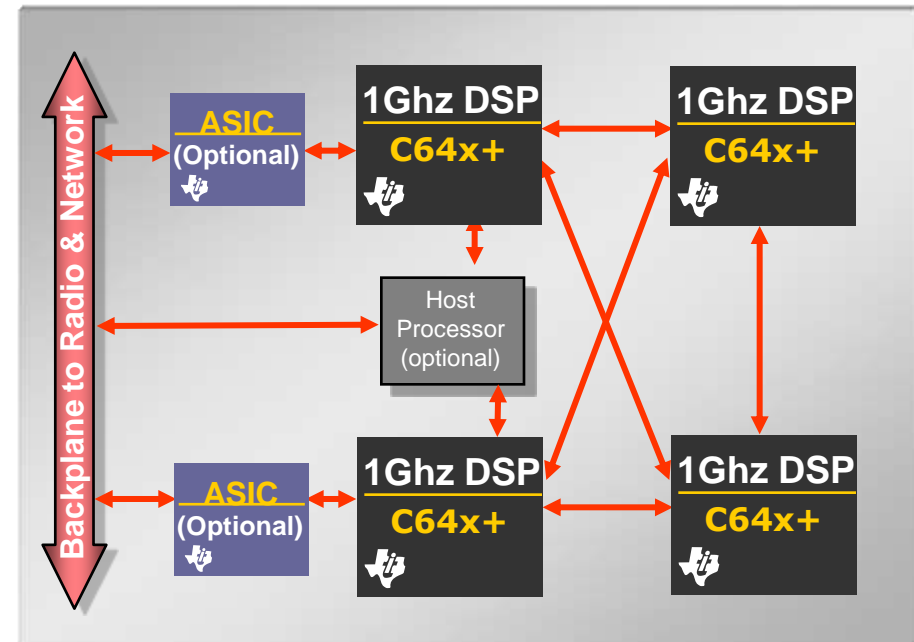
Baseband Applications



- Use of OBSAI/CPRI + RapidIO eliminates need for glue logic / bridge to seamless communicate to backplane
- Lowers total BOM cost

Improved DSP Interface with RapidIO

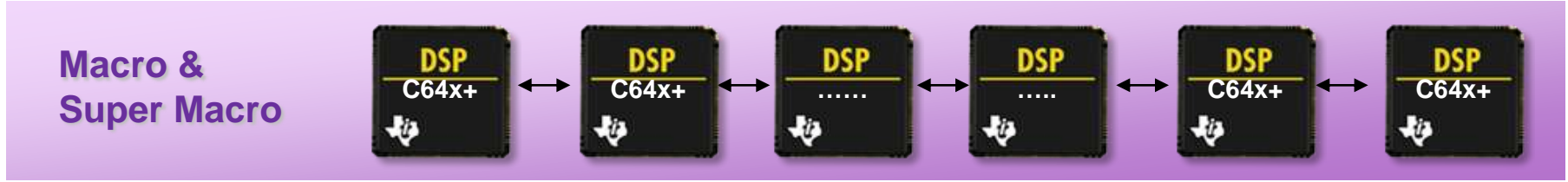
- Direct DSP-to-DSP interconnect with optional local Host / ASIC communication
- Used in complete baseband processor card
- ASIC used for custom applications
- Based upon MAC processing needed optional HOST processor is used



Multiple Form Factors Supported

- Easily Scalable
- One device for the entire product line
- Minimum board area, flexible solution

Aggregate Volume for Lower Cost



DSP < - > DSP links:	Serial RapidIO
Network link:	Integrated Ethernet

TCI6455

Faster Time-to-Market and Lower Development Cost

Features

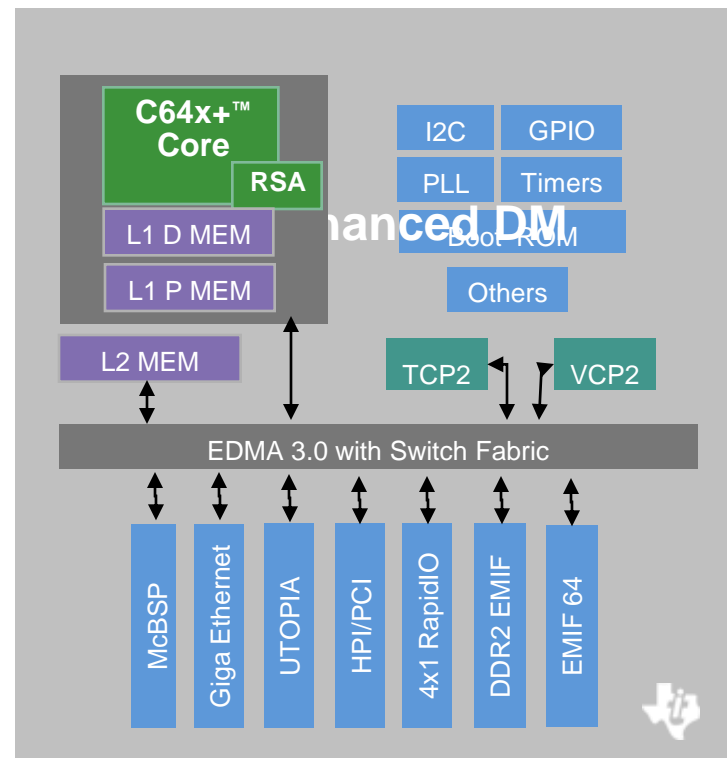
- **New C64x+™ Core**
 - C64x+ DSP Core at 1GHz
 - RSA instruction set extension for CR processing (uplink & downlink)
- **Memory**
 - 32 KB L1 program memory, 32 KB L1 data memory
 - 2 MB L2 memory
 - 32 KB Boot ROM
 - DDR2-533 MHz (32-bit) EMIF
 - 64-bit EMIF (synch/asynch)
- **Acceleration**
 - VCP2, TCP2
- **Peripherals**
 - 4x sRIO (1x links), or one 4x link
 - 10 / 100 / 1000 Ethernet – RGMII
 - 2x McBSP (serial ports), VLYNQ™
 - I²C, HPI, PCI – 66 MHz, UTOPIA II
- 90nm Process, ~ 3 watts
- 697 Pin, 24x24 FC-BGA, 0.8 Pitch
- **Production Now**

Benefits

- Power efficient base band processing
- Large on chip memory for faster application execution (Double L2 memory over current DSP)
- Single platform for multiple standards

Applications

- Baseband processor for WiMAX, W-CDMA, TD-SCDMA, GSM/EDGE, Edge Evolution
- MGW + Core network



TCI6474

Multi-Core Processor with Advance Accelerators

Features

■ C64x+™ Core

- Three (3) C64x+ DSP Cores at 1 GHz each
- 16-/32-bit ISA, doubled MPY vs. C64x™ core
- RSA instruction set extension for CR processing (downlink & uplink)

■ Memory

- 32 kB L1 program memory, 32 kB L1 data memory
- 3 MB of total L2 memory (2 configurations)
1MB / 1MB / 1MB or 1.5MB / 1MB / 0.5MB
- Boot ROM, DDR2-667 MHz (32-bit)

■ Acceleration

- VCP2, TCP2

■ Peripherals

- 2x sRIO (1x links)
- 10/100/1000 Mbps Ethernet – SGMII
- Antenna interface supporting OBSAI / CPRI – 6 links
- McBSP (TDM)

■ 65nm Process

■ 561 Pin, 23x23 mm FC-BGA, 0.8 Pitch

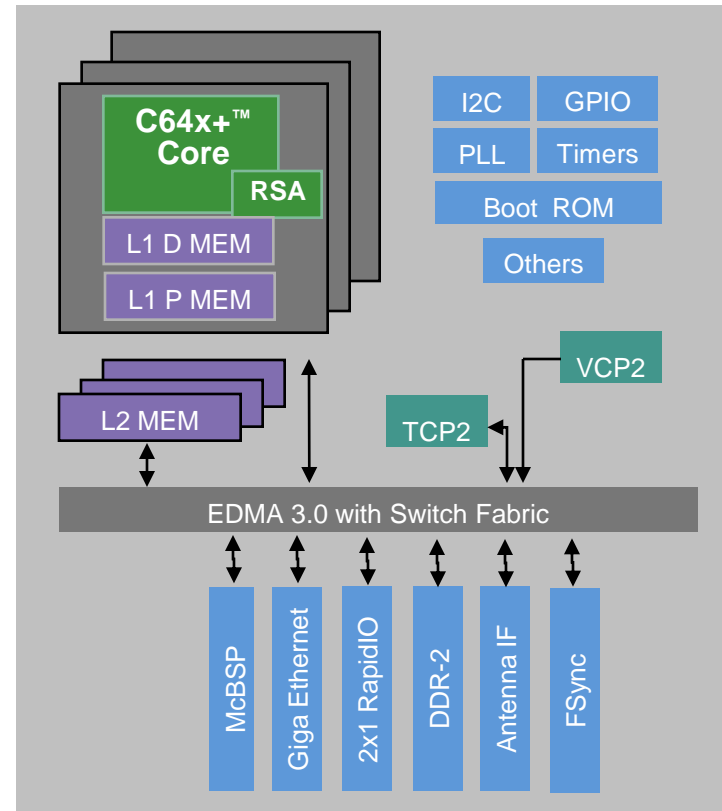
■ Schedule: In Production Now

Benefits

- 3 GHz of raw performance
- SmartReflex to minimize power consumption
- Board level efficiency by utilizing industry standard IF standards (sRIO, OBSAI, CPRI, DDR-2 memory, etc.)

Applications

- Pico and macro base station
- Higher capacity or increased bandwidth requirements for baseband cards
- Baseband processor for WiMAX, W-CDMA & TD-SCDMA



Summary & Conclusion

- Communication Infrastructure applications require a serial interconnect
 - **Driven by need for low pin count, backplane connectivity and bandwidth scalability**
- For embedded system applications, RapidIO is the best technical choice
 - **Peer to Peer Connectivity & Switch Fabric Capability**
 - **Performance/Flexibility**
 - **Support of embedded players**
 - **Rich choice of speeds and widths**
- RapidIO has gained momentum with silicon vendors and end equipment manufacturers.
- TI is committed to supporting RapidIO in all Wireless Infrastructure DSPs
 - **RapidIO is strategic to TI's Communications Infrastructure roadmap**

Q/A