



Tundra Semiconductor: Developing Wireless Base stations in MicroTCA Systems with RapidIO AMCs

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TUNDRA CONFIDENTIAL



1. RapidIO Overview
2. RapidIO and MicroTCA Overview for Wireless
3. Basestation design with AMCs
4. 3G Baseband Processing Evolution for Cost Reduction

- Industry-leading public fabless semiconductor company focused on System Interconnect products, Design Services and IP – since 1995
- Headquarters in Ottawa, Ontario, Canada
 - Design centers in Canada, US & India
 - Design services division - Silicon Logic Engineering, Inc.
 - Sales offices throughout North America, Europe & Asia
 - ~240 employees
- FY08 Results to Date (Q1 and Q2)
 - Revenue FY08 YTD \$38M
 - Pro Forma Earnings FY08 YTD \$2.9M
 - Diluted Pro Forma Earnings per Share \$0.14
 - Positive Pro Forma Earnings, 21 consecutive quarters
- Global Customer Base
 - Approximately 50% of revenues come from global Tier 1 customers
 - First class customer service and support
- Strong R&D Investment
 - 30% of sales in FY 07



Chips, Boards, Backplanes and Beyond...



1GHz, 2.5GHz, 3.125GHz, 5GHz, 6.25GHz...



1X, 2X, 4X, 8X, 16X...



Load/ Store, Memory Mapped, Message Passing, Flow Control...



IP, FPGA, ASIC, Standard Products, DSP's, CPU's...

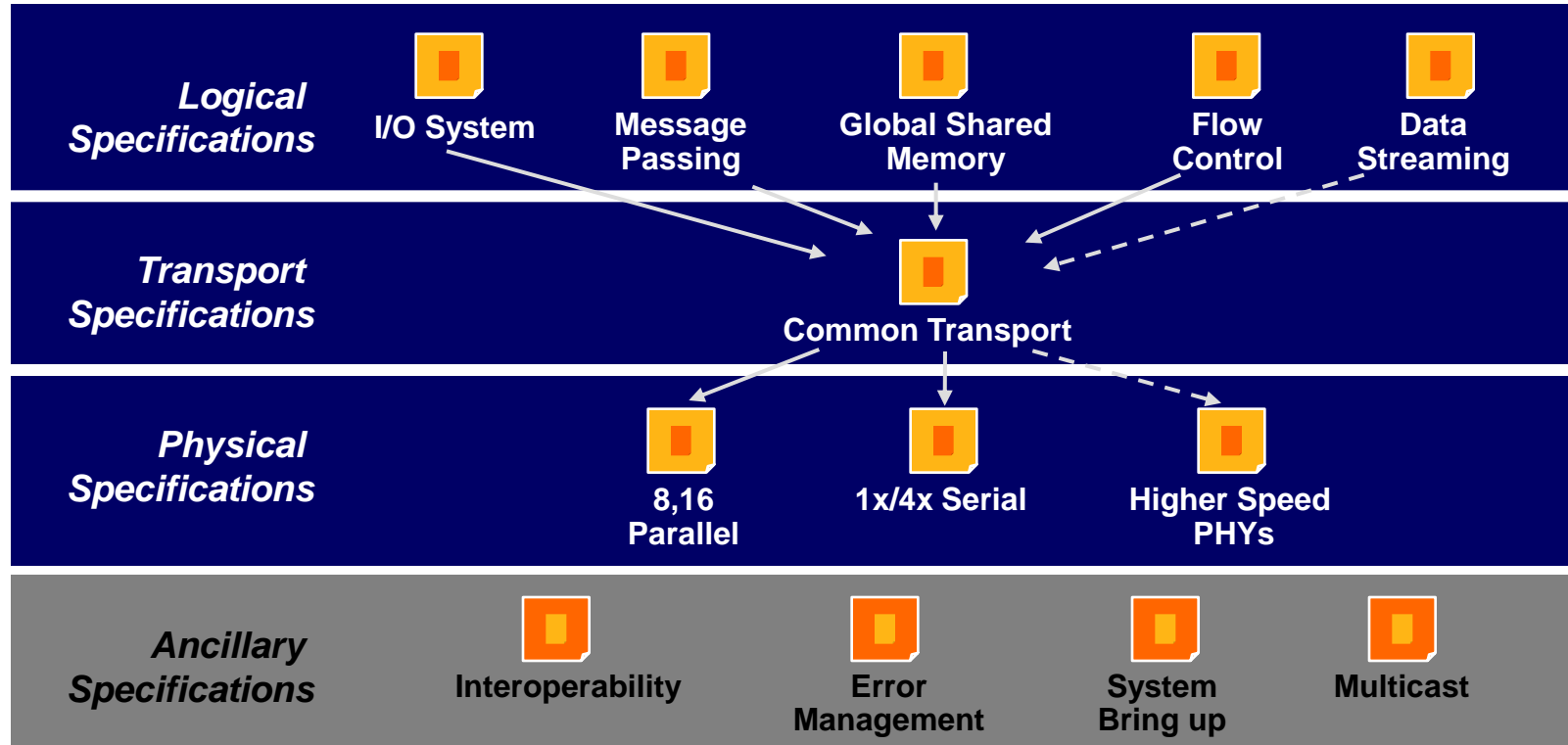


RTA Steering Committee Members

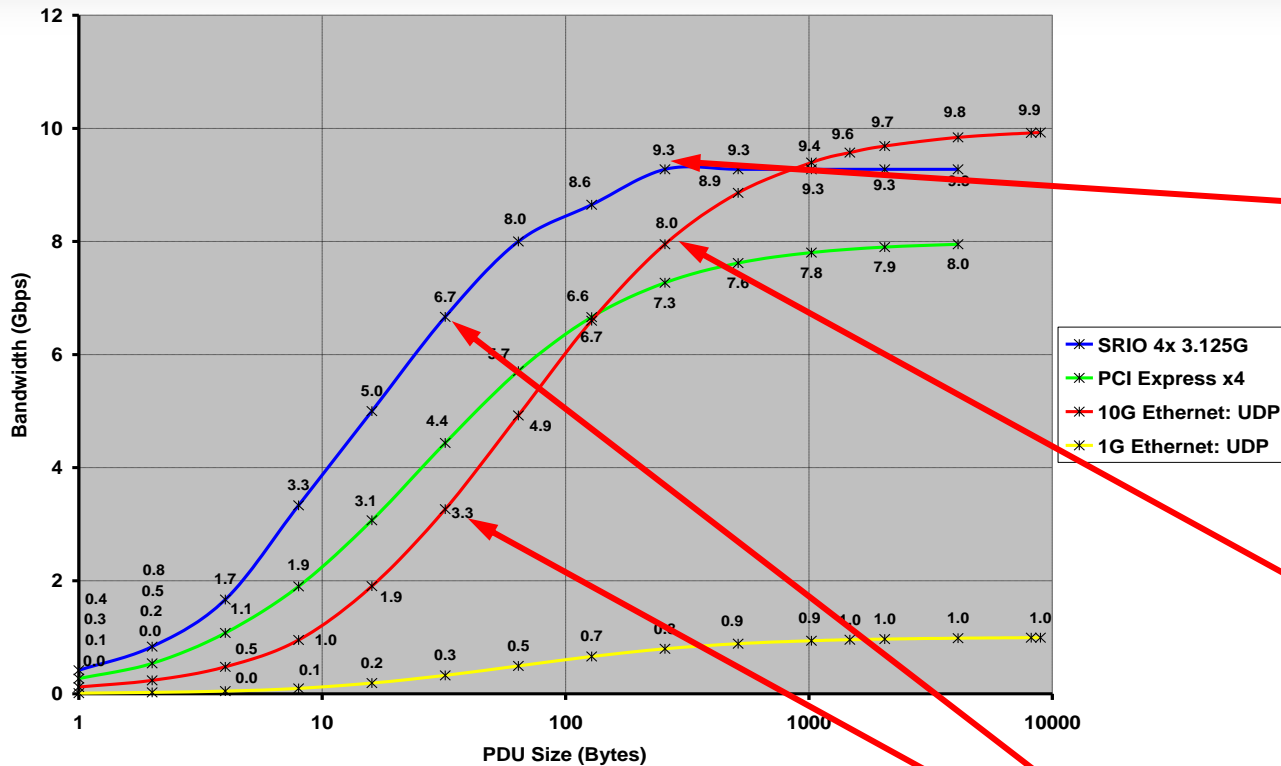




Application Requirements	Wireless	Military	Medical	Video
Scalability	✓	✓		✓
Fault Tolerant	✓	✓	✓	✓
Peer-to-peer	✓	✓	✓	✓
Independent memory systems	✓	✓	✓	✓
Messaging	✓	✓	✓	✓
Low Latency	✓	✓	✓	✓
Redundancy		✓	✓	
Multicast	✓	✓	✓	✓



3-layer protocol terminated in hardware
 ideal for peer to peer multi processor
 systems with high speed signaling and low
 latency



RapidIO
9.3 Gbps
actual data rate
256 byte PDU

10 GbE
Only ~8Gbps

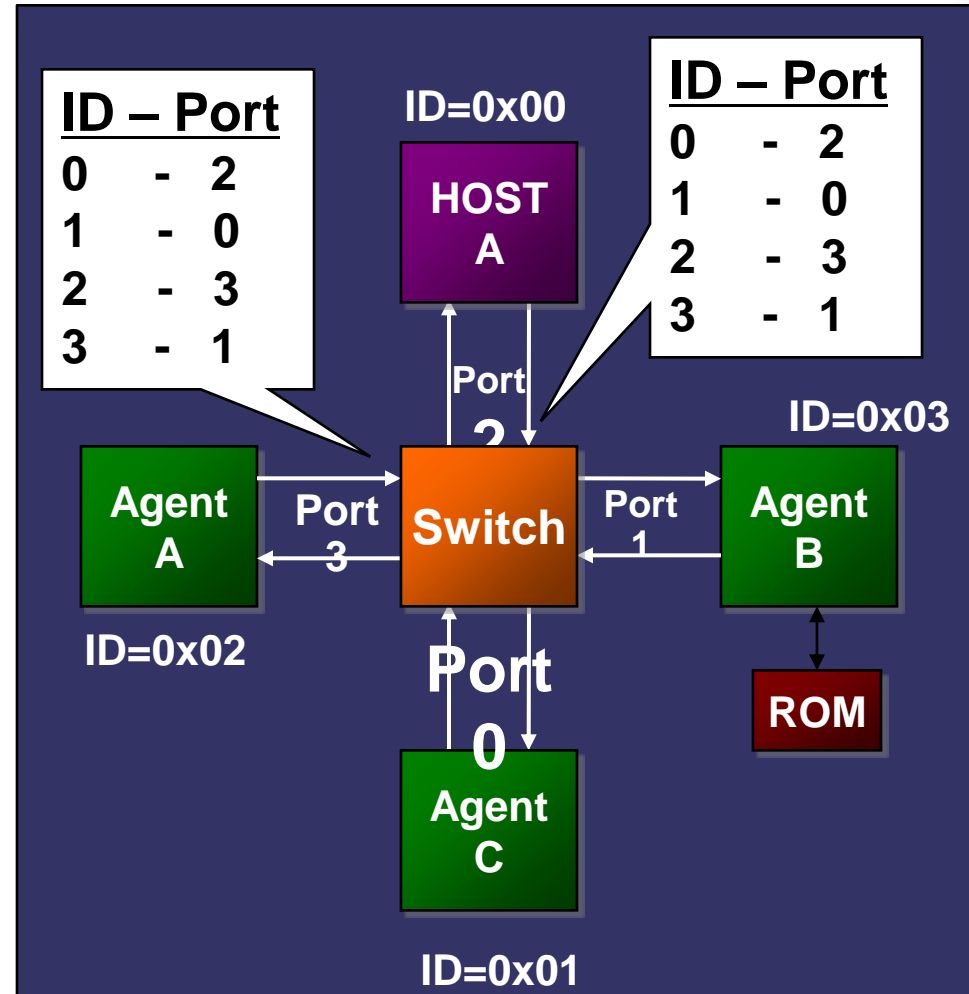
For smaller
packets sRIO
doubles
10GbE

- Scalable Bandwidth from 1-10 Gbps of data rate after 8/10b encoding
- >95% efficiency of protocol: supporting data intensive applications such as WiMAX, 3G LTE
- GbE only provide 795Mbps of effective data rate on 256byte PDU
- 10 GbE provides only 3.3 Gbps at small 64 byte PDU vs 6.7 Gbps for sRIO

- Architecture can grow depending on the application
 - E.g. Pico, Micro and Macro Base Station
- Serial RapidIO offers multiple baud rates
 - One architecture can be reused for similar application with different speed grades up to 6.25 Gbaud with sRIO 2.0
 - Motherboards can have mezzanine cards for added processing power to accommodate larger systems
- Serial RapidIO protects your SW investment

Clock Rate	1 bit wide			4 bit wide		
	PEAK	Sust 32B Op	Sust 256B Op	PEAK	Sust 32B Op	Sust 256B Op
1.25 GHz	1 Gb	0.5 Gb	0.9 Gb	4 Gb	2 Gb	3.6 Gb
2.5 GHz	2 Gb	1 Gb	1.8 Gb	8 Gb	4 Gb	7.2 Gb
3.125 GHz	2.5 Gb	1.25 Gb	2.25 Gb	10 Gb	5 Gb	9 Gb

- RapidIO networks are built around two “Basic Blocks”
 - Endpoints
 - Switches
- End points source and sink packets
- Switches pass packets between ports without interpreting them
- Simple routing through Look Up Tables
- Typical Switch Latency is 100-150ns



Requirements: Peer to Peer & Independent Memory System

- Routing is easy: Target ID based
- Every endpoint has a separate memory system

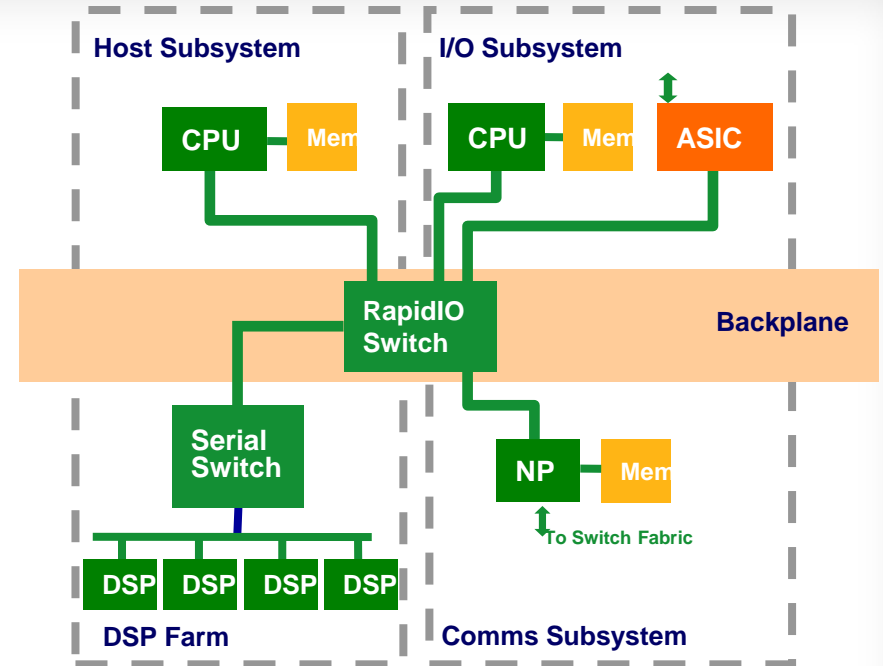
	1	3	1	1	2	2
Prev Packet	S	AckID	Rsrv	S	Rsrv	Prio

2	8 or 16	8 or 16	4
TT	Target Address	Source Address	Transaction

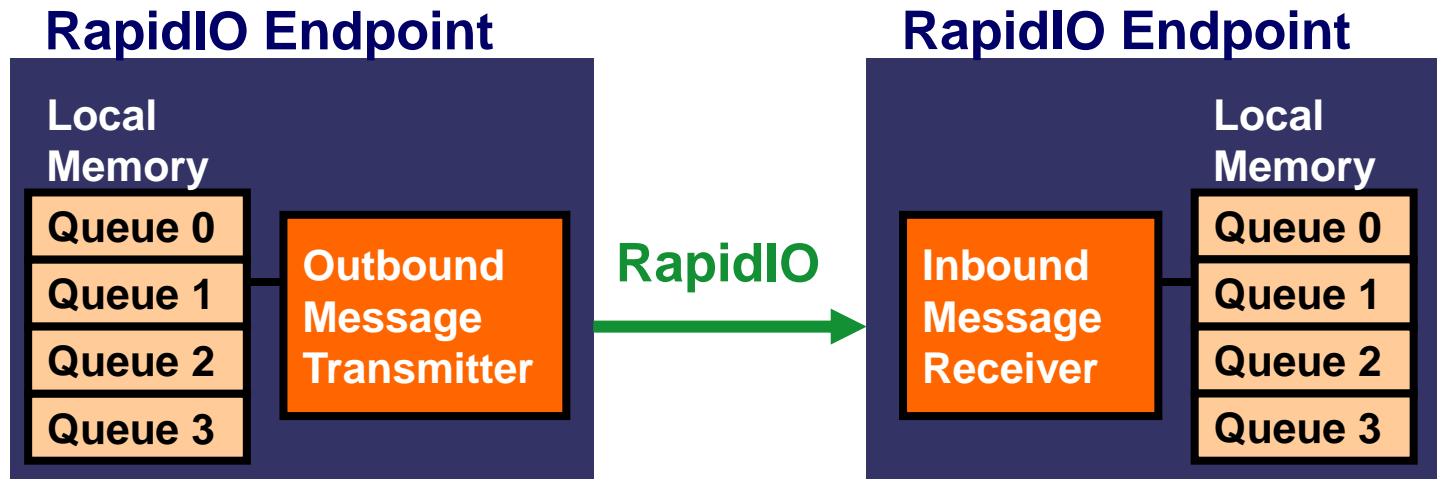
4	4	8	32 or 48 or 64
Ftype	Size	Source TID	Device Offset Address

8 to 256 Bytes	16	
Optional Data Payload	CRC	Next Packet

Physical
 Transport
 Logical

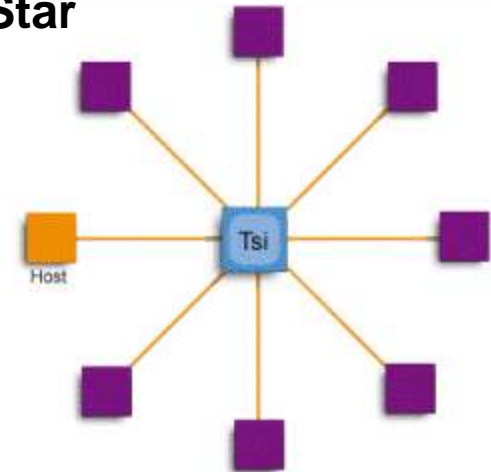


- Messaging uses a push architecture
- Receiver is responsible for storing the message in its memory system
- Overall system latency per message transfer is reduced significantly

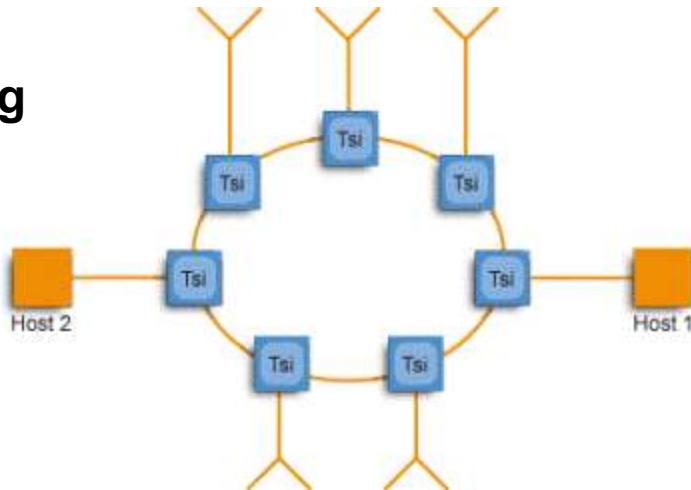


- All topologies are supported
 - Star and Dual Star
 - Full Mesh
 - Ring
- Redundancy can be supported in HW and or SW

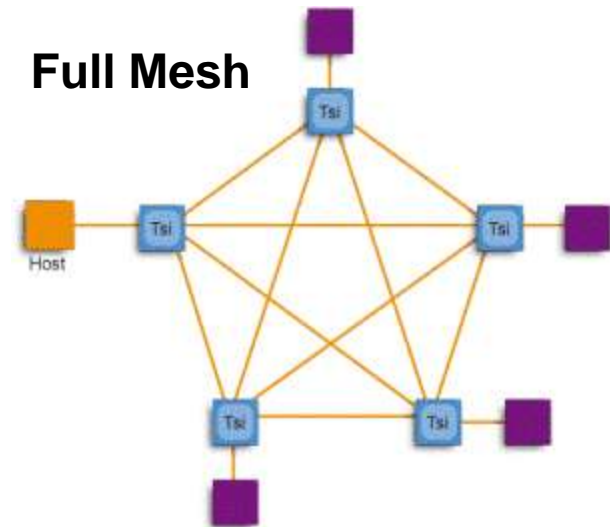
Star



Ring



Full Mesh





● DESIGN
● CONNECT
● GO

MicroTCA™ Baseband Systems with RapidIO



- RapidIO is an ideal protocol for the following:
 - Embedded Systems
 - Peer to Peer Communications
 - Multiple Distributed processing environment
 - Low latency
 - Large number of discrete processors, FPGA's, ASICs and DSPs requiring large amount of transmitted data

- Interconnect is needed in MicroTCA systems on:
 - Backplane
 - MicroTCA Carrier Hub Switch Card which provided interconnect between AMC's
 - AMC Cards for chip to chip interconnect

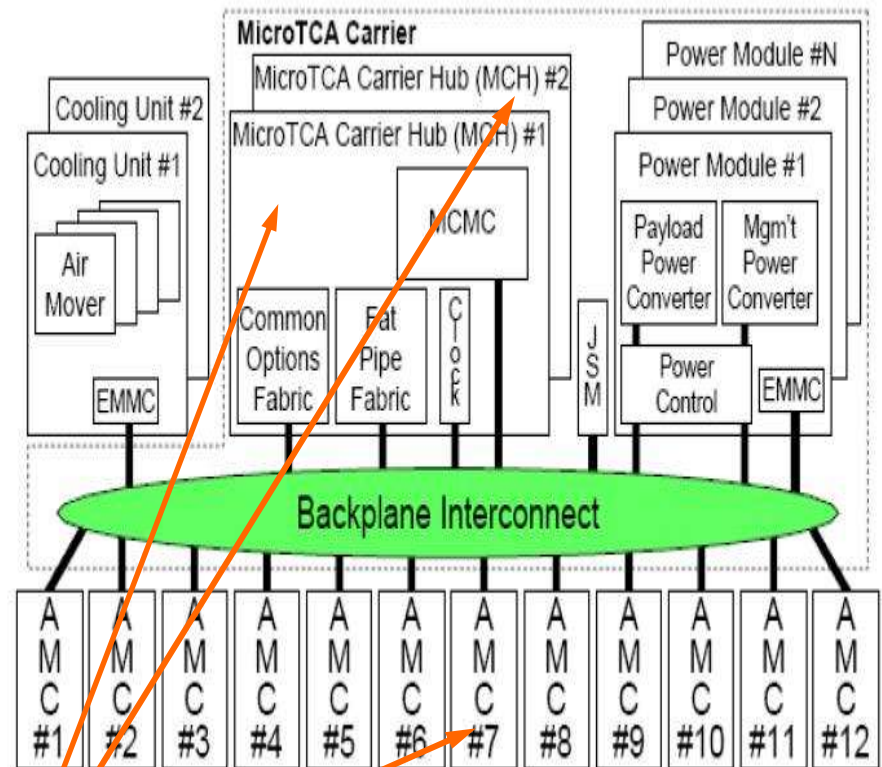
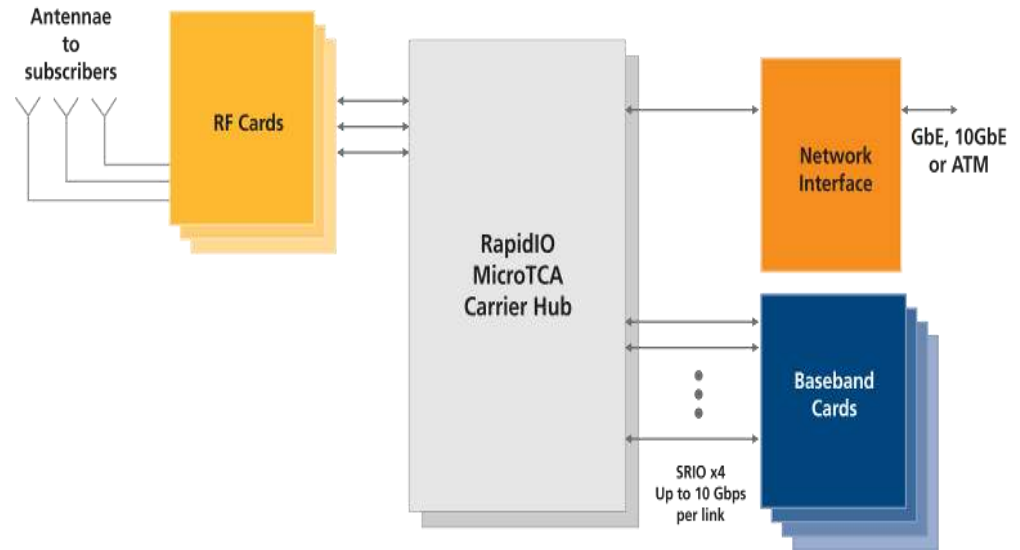
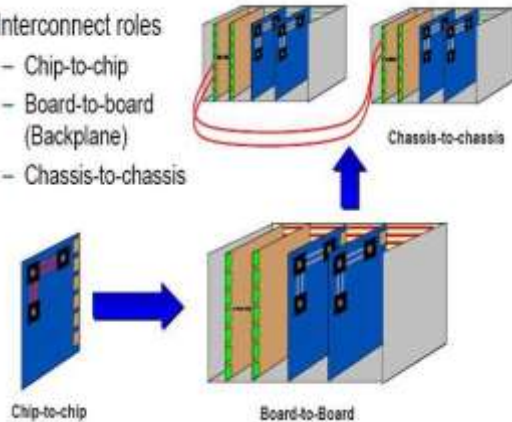


Figure Copyright PICMG

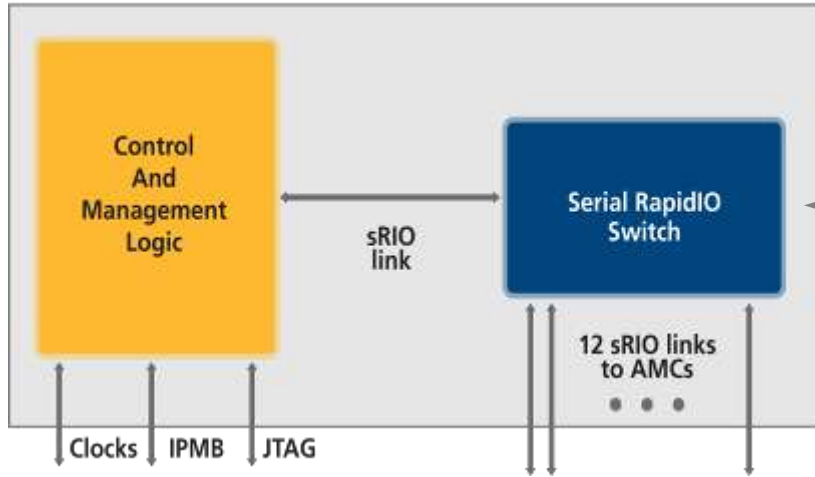
RapidIO Interconnect on Backplane, MCH and AMC's

- Interconnect roles
 - Chip-to-chip
 - Board-to-board (Backplane)
 - Chassis-to-chassis



Key Elements

- Antennae provide interface to mobile or fixed subscribers
- RF cards convert analog RF signal to digital “chip rate” data
- RapidIO-enabled MCH takes chip rate from each antenna and forwards to all baseband cards
- RapidIO-enabled baseband cards pull symbol rate data out of chip rate data, and forward processed data to network interface
- RapidIO-enabled MCH forward data to other baseband cards or to the network



- Switch with up to 10 Gbps of bandwidth per link, connectivity to AMCs
- Optional switch cluster
- MCH provides control and management infrastructure as well as switching
- Since MCH provides a shared resource and can be a single source of failure, high availability systems may require dual MCH

- Designed by Ericsson for MicroTCA platform
- Available to multiple vendors via sublicense from Tundra Semiconductor
- Supports 12 high bandwidth 10G Serial RapidIO ports featuring Tsi578 Switch
- 10 Gbps sRIO on Front Panel
- High signal integrity across backplane



- NAT Europe upgraded their existing MicroTCA MCH design to use RapidIO
- NAT has the following “fat pipe support”
 - Serial RapidIO
 - PCI Express
 - 10 GbE Xaui
- Target Markets
 - Wireless
 - Military
 - Video
 - Medical





AMC .4 Support



X4 sRIO to backplane @3.125 Gbaud

Signal Integrity



Signal Analyser, Ball Map, SerDes

Cut Through Latency



110ns in x4 @3.125 Gbaud

Traffic Shaping



Programmable Buffers by priority per port

Non Blocking



80 Gbps of non blocking bandwidth

Field Proven

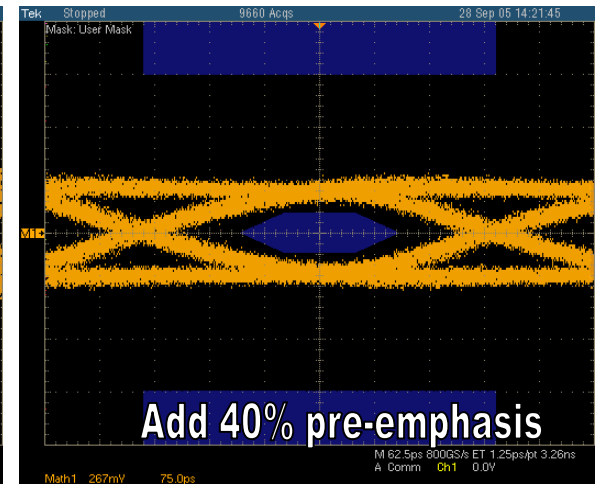
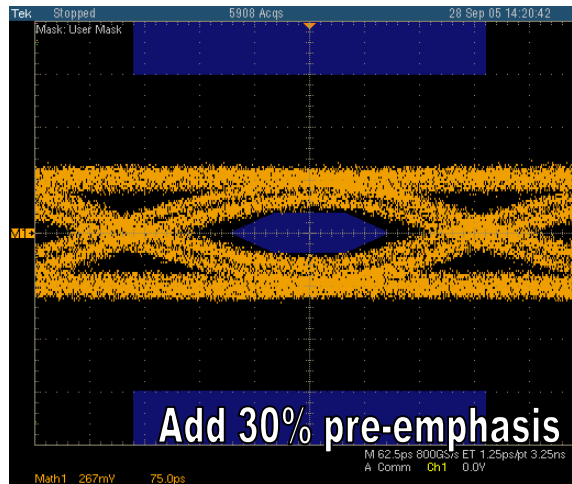
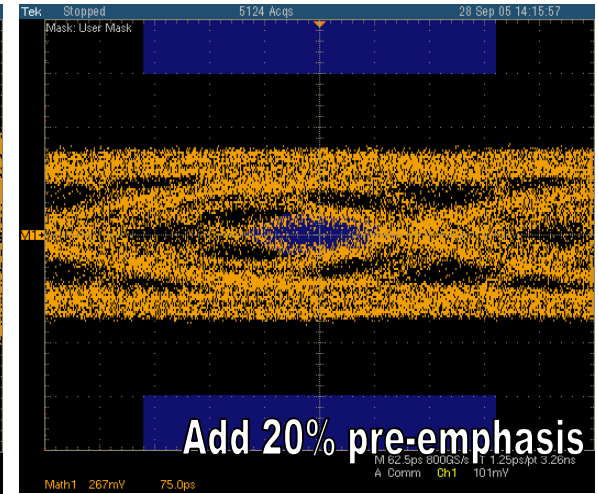
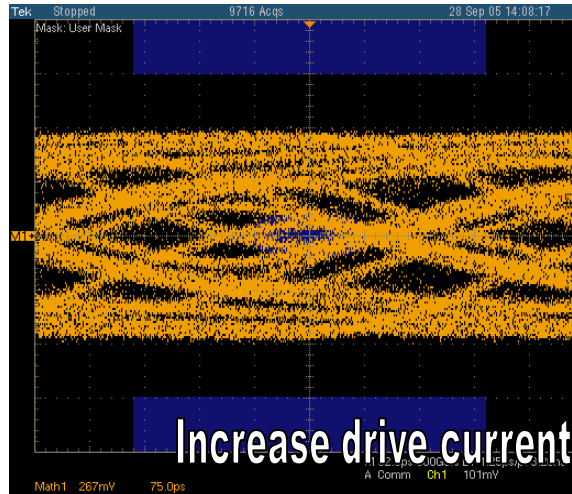
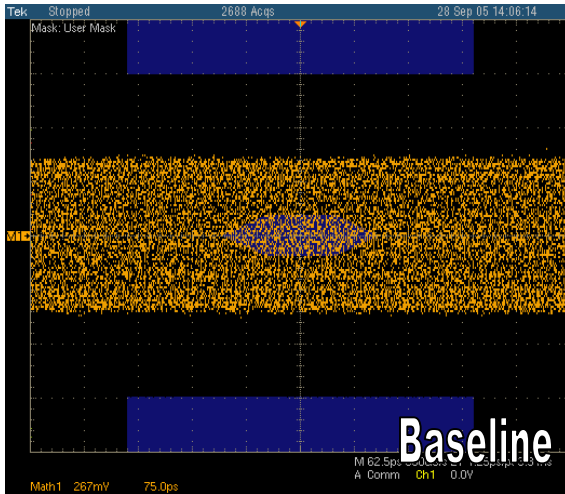


Mercury and NAT MCH options

Future Proof

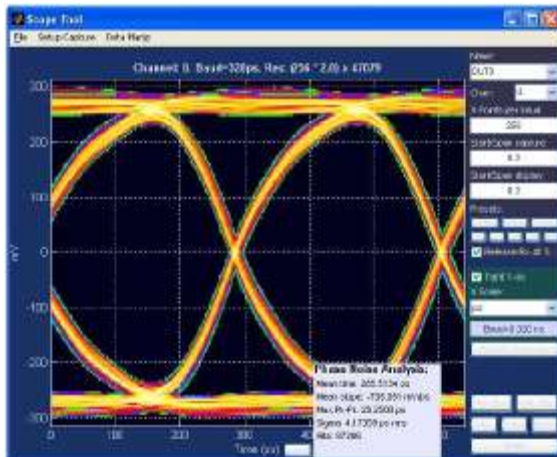


Migration Strategy to sRIO 2.0 for performance and cost reduction



**4 Lanes
3.125 Gbaud
10 Meter Cable!**

- AMC Form Factor Card
- Manage eye as seen on die with no scopes
- Critical to switch Card development
- Adjust pre emphasis and receive equalization on a port by port basis via software



Basic Control and Status Report for ALLPHY Test Diag Rev 1.0.0

Common Controls

Reset and Reload Refresh GUI

BERT Pch: LFSR7 BERT Pch: LFSR7 Sync Pch

Phy Clk (MHz): 100.00 Baud Rate (GHz): 3.125 Duplexes: 1 0, 2 0

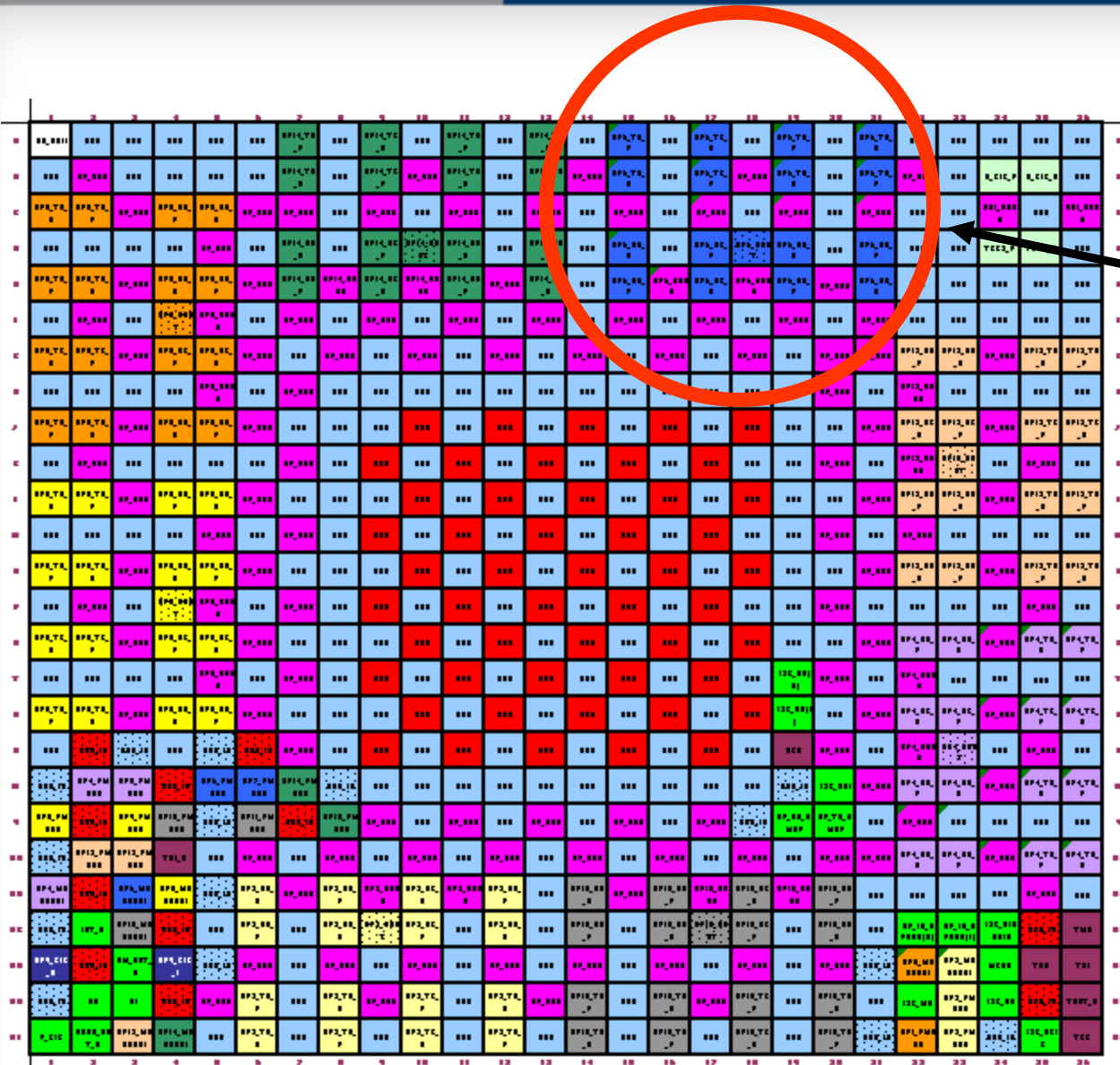
Tx Level (pwrB/dBm): 1903 Tx Attn: none Tx Tx Lin (pwrB/dBm): 1903

Tx Boost (dB): 2.7 Rx Supr (dB): 1 Rx Opt: low, post, pre

Full Rate:

Per lane controls and status					
OUT0	TXRX	POLARITY	LINK STATE	BIT ERROR RATE	
0	ON	FUPPED	FROZEN		
1	ON	FUPPED	SYNCH	0/1.1e+005	0/1.1e+005
2	ON	UNKNOWN	LOS		
3	ON	UNKNOWN	LOS		

Per lane controls and status					
OUT1	TXRX	POLARITY	LINK STATE	BIT ERROR RATE	
0	ON	FUPPED	SYNCH	0/9.1e+005	0/9.1e+005
1	ON	FUPPED	SYNCH	0/6.5e+005	0/6.5e+005
2	ON	UNKNOWN	LOS		
3	ON	UNKNOWN	LOS		



x4 sRIO Port with lane separation for superior signal integrity

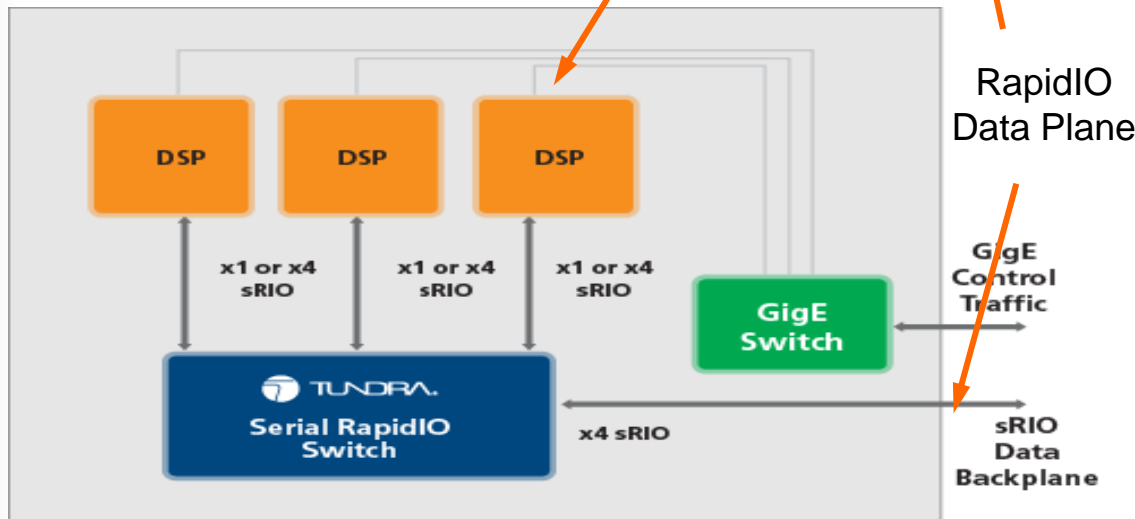
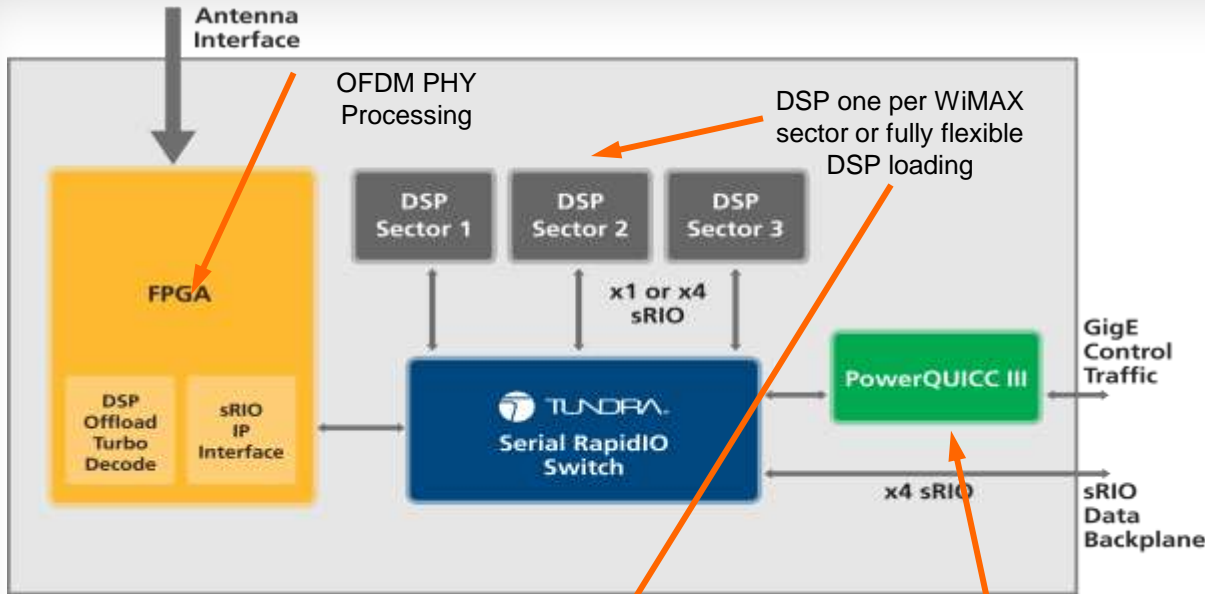
1. Blue = Signal
2. Light Blue = Power
3. Violet = Ground



● DESIGN
● CONNECT
● GO

RapidIO Baseband Cards





- Higher data rates in WiMAX than 3G requiring more backplane bandwidth
- Can use GigE in control plane on backplane, merged backplane on card
- One DSP per sector or fully flexible DSP loading
- Antenna data terminated in FPGA for OFDM processing on ATCA Card, on daughtercard for AMCs
- PQIII does control and Mac layer processing which is very CPU Intensive for OFDMA
- Same architecture can be leveraged for “pizza box” pico and microcell coverage

Tundra Based RapidIO AMCs



Commagility AMC
Tsi578, XilinxV4, TCI6455

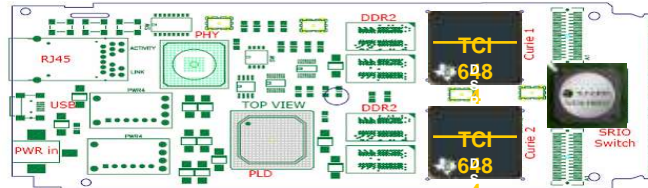


Commagility AMC
Tsi578, XilinxV4, TCI6487



Mercury Computer Systems, Inc
MTI-203

Mercury MTI 203 with
Tsi578, XilinxV4, TCI6482



Tsi 574 and TI 6484 (Curie)



Tsi 578 + FSL8144 DSP



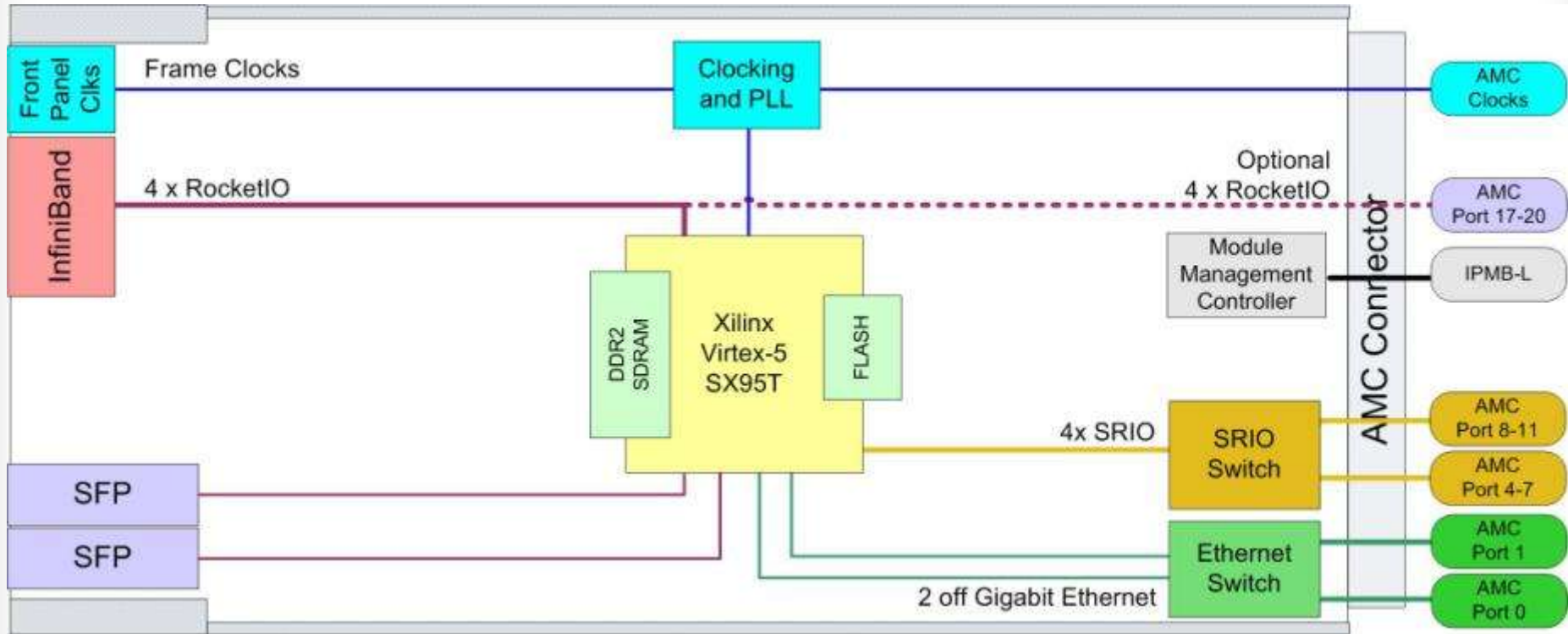
Tsi 578 MSM
(MicroTCA Switching)



Tsi 620 EVB with
TCI8487 DSP

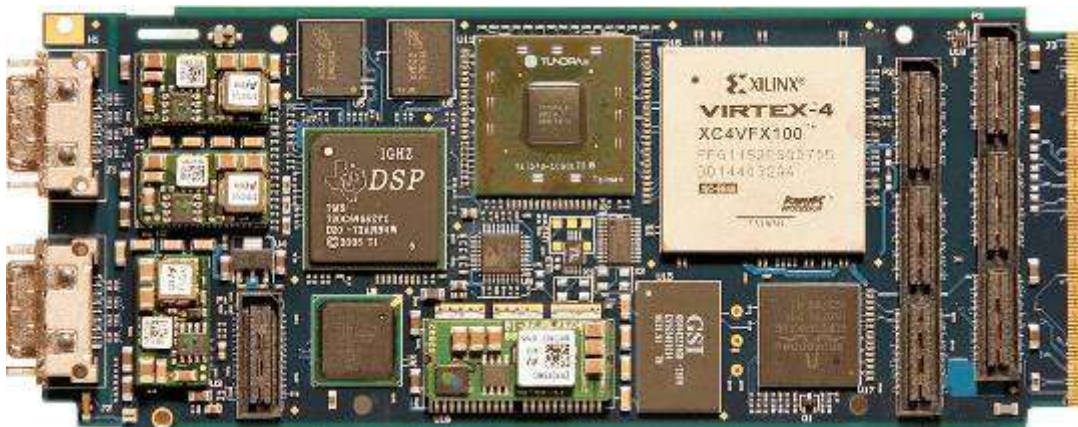


FSL 8548 RapidIO AMC



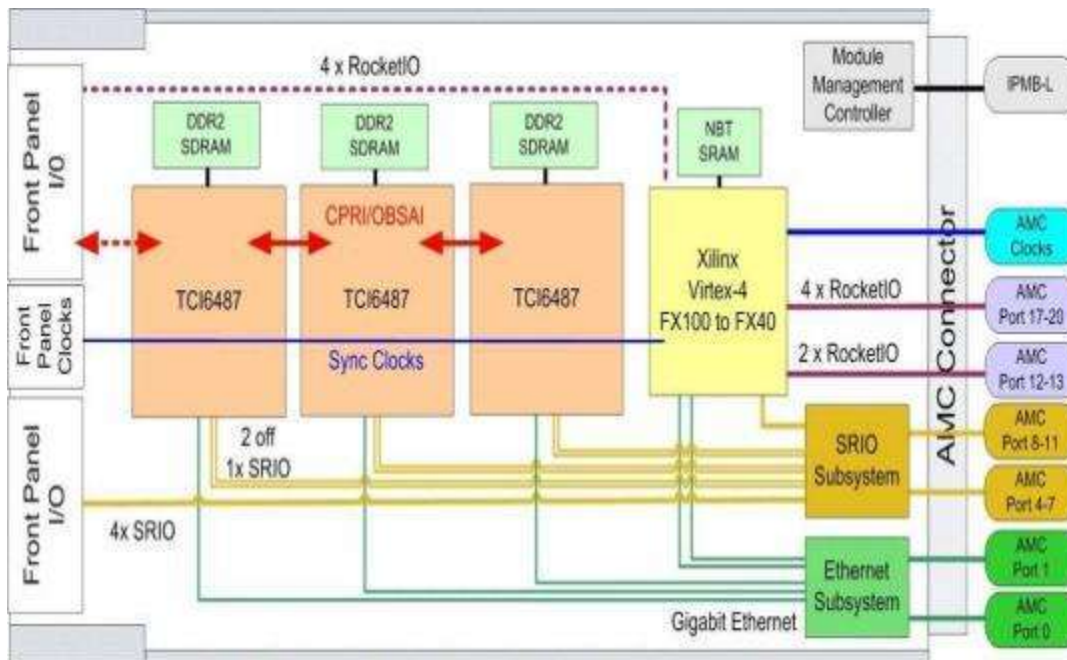
- Mid or Full size AMC (frame clocks on full size only)
- FPGA options e.g. SX95T, LX110T, LX155T, FX100T
- Launch Q4 2008

- Baseboard + Mezzanine architecture maximises use of single full-size AMC slot
- 4 x TI C6455 @ 1 or 1.2 GHz each with up to 256MB SDRAM
- Xilinx Virtex-4 FX-100 with up to 18MB NBTRAM
- High bandwidth DSP EMIF to FPGA buses
- Tundra Tsi578: Full 10Gbps SRIO to card devices, AMC fabric, front panel
- Broadcom BCM5389: Gigabit Ethernet to card devices, AMC fabric
- Virtex-4 RocketIO to AMC connector and front panel



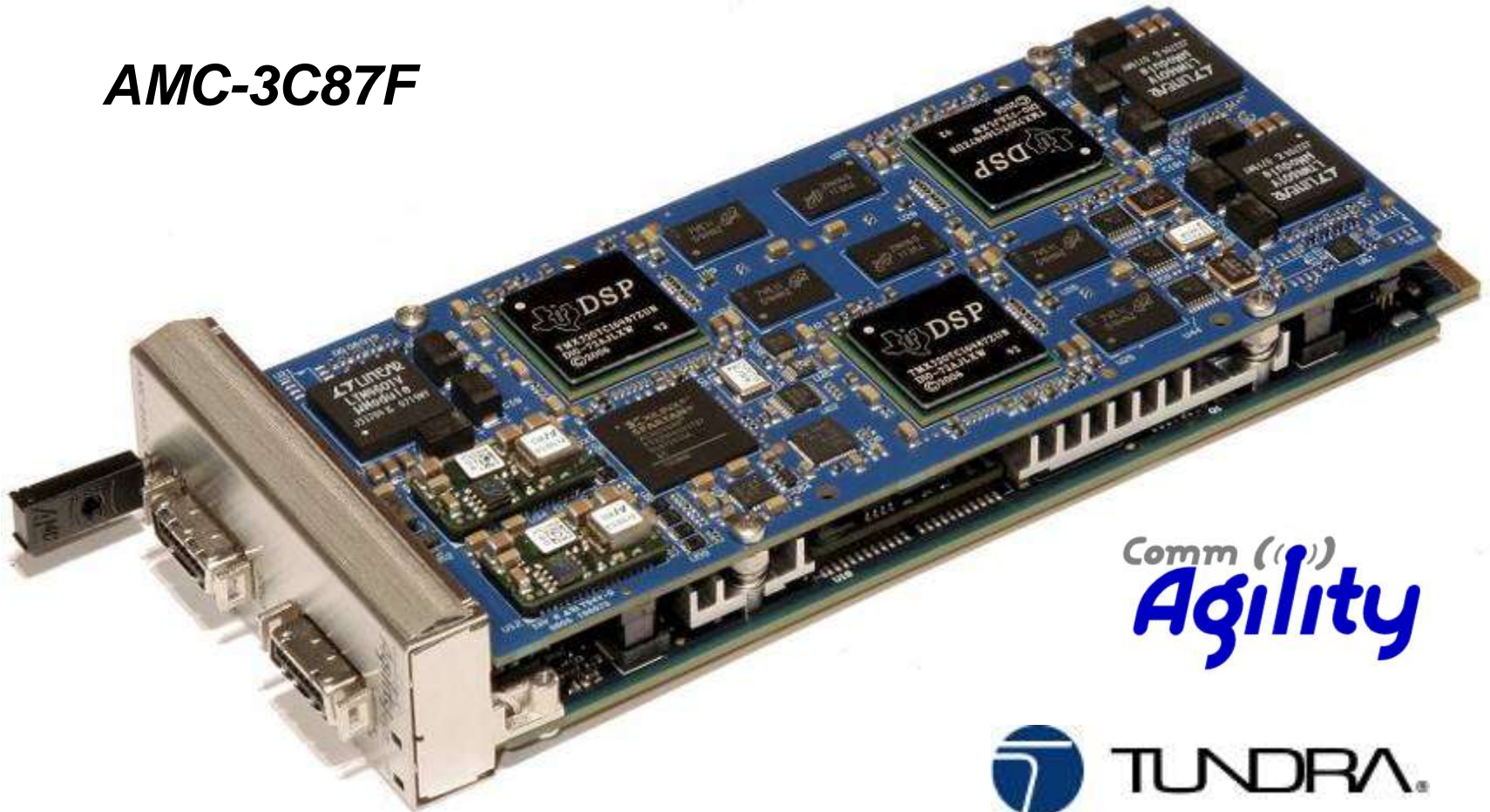
Comm (())
Agility

AMC-3C87F



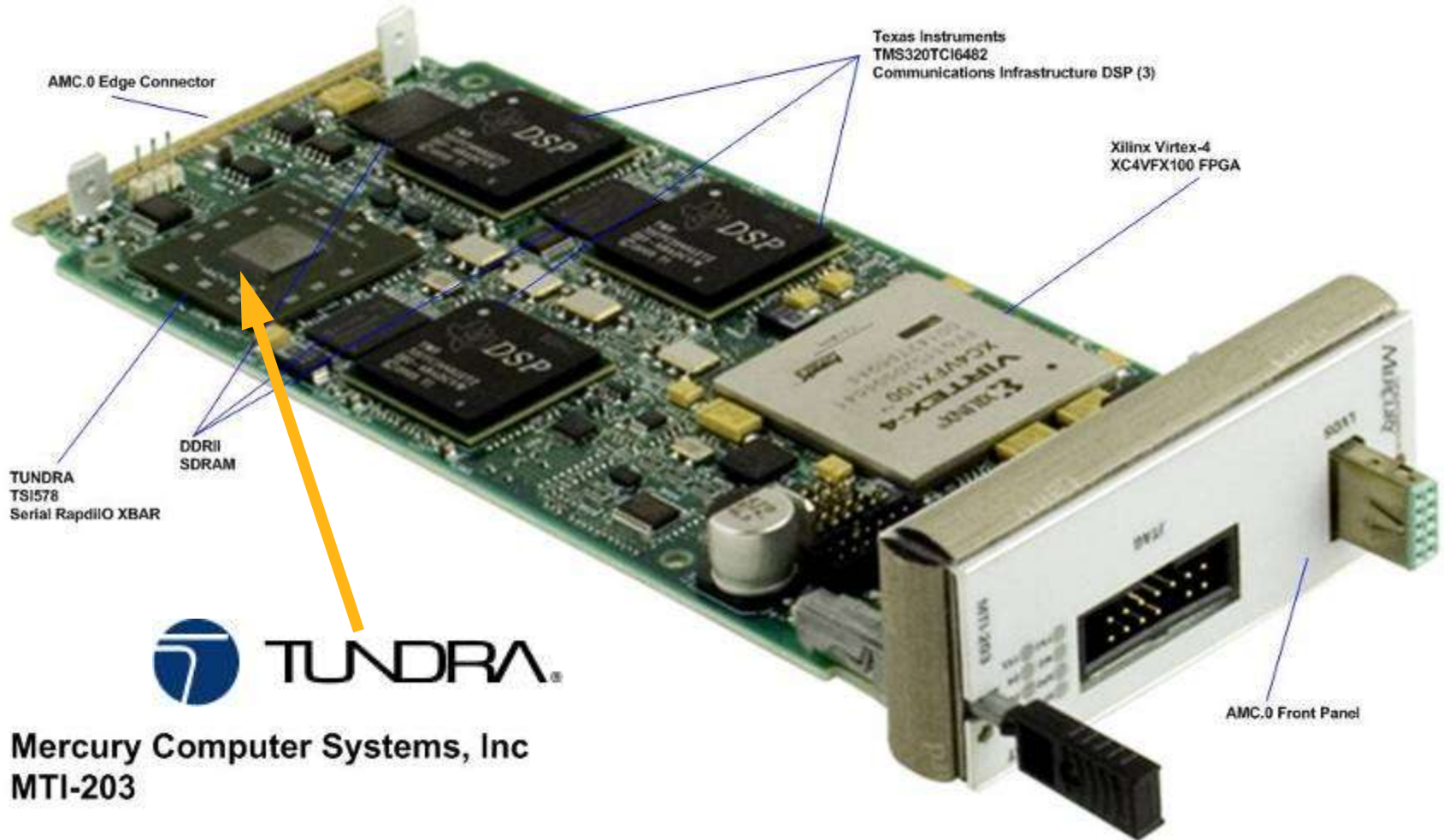
- Full use of 8 port Tundra Tsi578 sRIO switch:
 - Two 4x 10Gbps SRIO ports to AMC backplane: 4-7 and 8-11
 - Four 4x 10Gbps SRIO ports to DSPs, one to each
 - One 4x 10Gbps SRIO port to FPGA for Xilinx SRIO IP core
 - One 4x 10Gbps SRIO port to front panel: “InfiniBand-type” connector with standard cables available.

AMC-3C87F



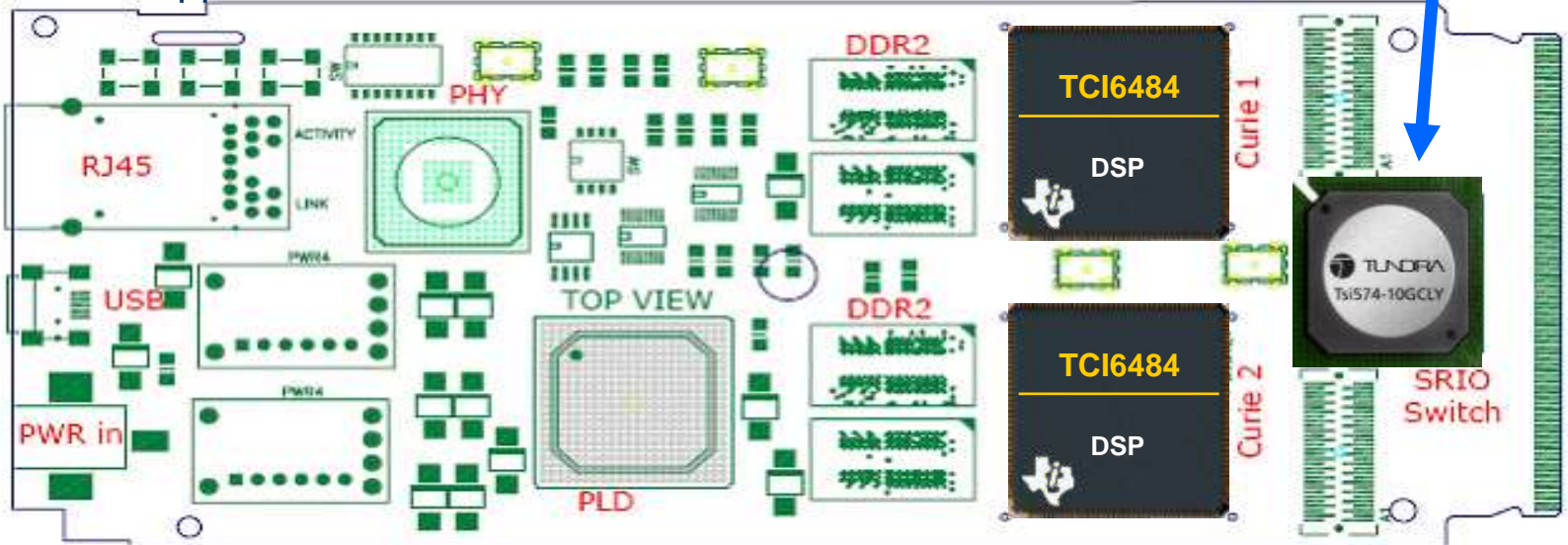
Comm (())
Agility





Mercury Computer Systems, Inc
MTI-203

- AMC Compatible Card -- Single Wide
- Two TCI6484 DSPs
- DDR 256MBytes @ 667MHz per Curie (2 64Mx16 per Curie)
- ClockIn support:: 1.0Ghz (Default)
- RapidIO with Tundra Tsi574 Switch
 - Supported on AMC connector
 - SRIO supported between Curie1 & Curie2 with Tundra Tsi574
 - Configurable line rates for 1.25, 2.5, and 3.125 Gbps
- SGMII Supported via RJ45 and between Curie1 & Curie2

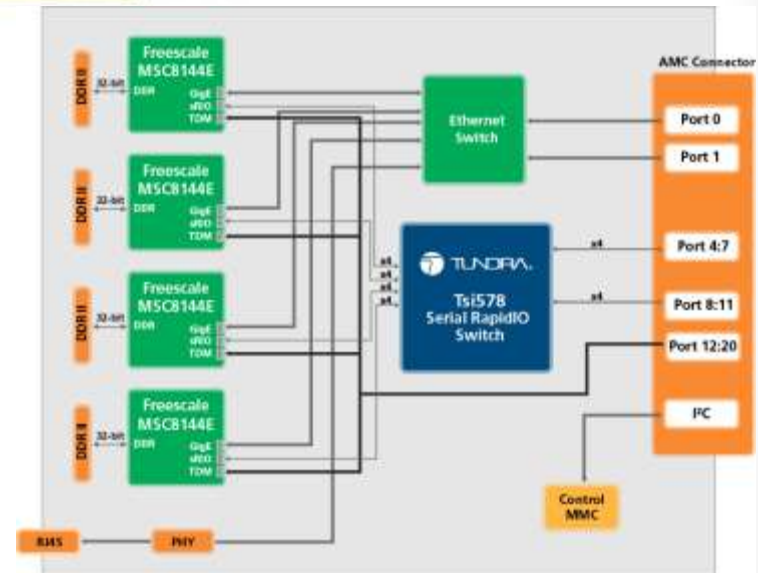




Joint Platform for Rapid Prototyping in an AMC Form Factor:

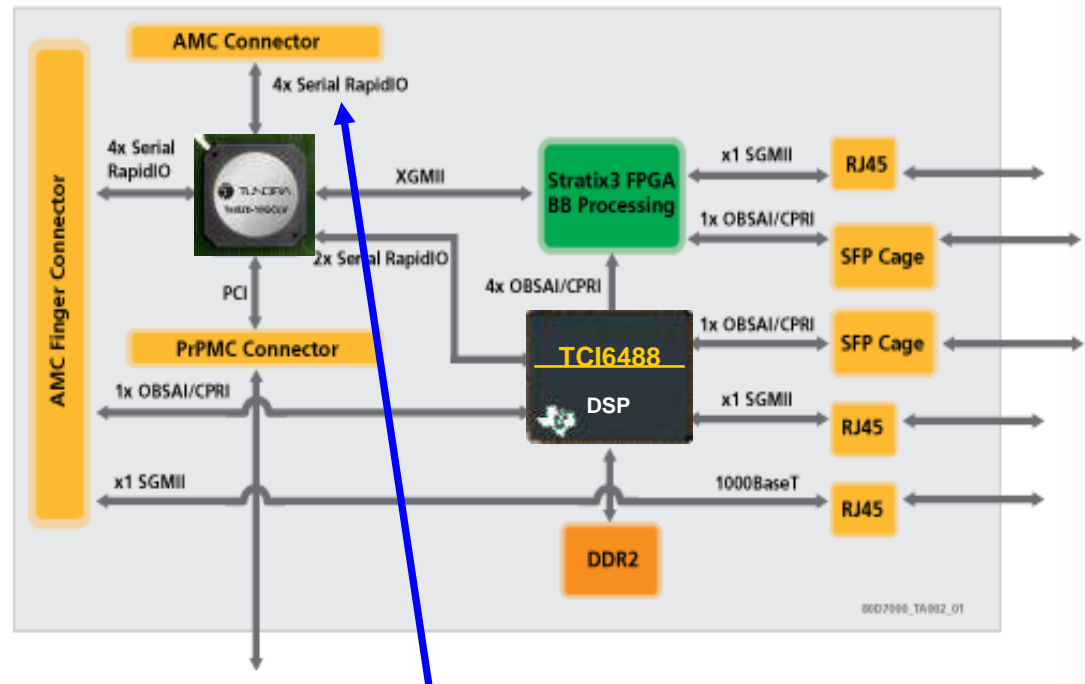
- Four Freescale MSC8144E quad core DSPs
- Serial RapidIO interconnect using Tundra Tsi578 Serial RapidIO Switch
- Per port bandwidth up to 10 Gbps
- Ethernet switching for control plane
- Powered via AMC connector

Applications: WiMAX, 3G LTE, Video, Media Gateway



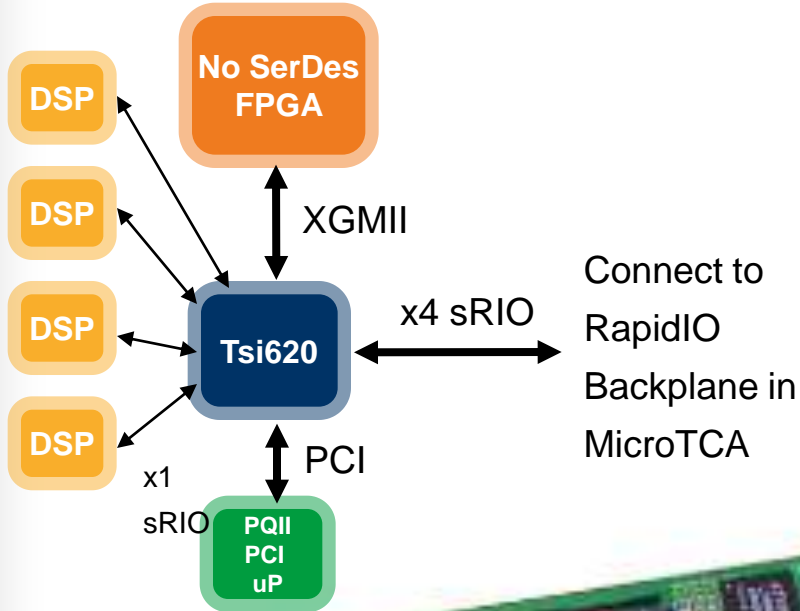
Key Features:

- AMC width board usable in uTCA
- Can be used in Standalone Mode
- Tsi620 Multi Protocol Switch
- On board TI Faraday TCI6488
- Altera Stratix3 FPGA running RapidIO over XGMII to Tsi620
- Antenna interface to FPGA and DSP
- RapidIO 2x1 from Tsi620 to TCI6488
- RapidIO x4 to backplane and AMC finger connector
- Hardware bridging to PCI, PCI interface exposed to PMC connector
- DSP cluster extendable via backplane RapidIO to CommAgility Triple Faraday DSP AMC using RapidIO
- Ethernet connectivity to FPGA and DSP available through RJ45 connectors



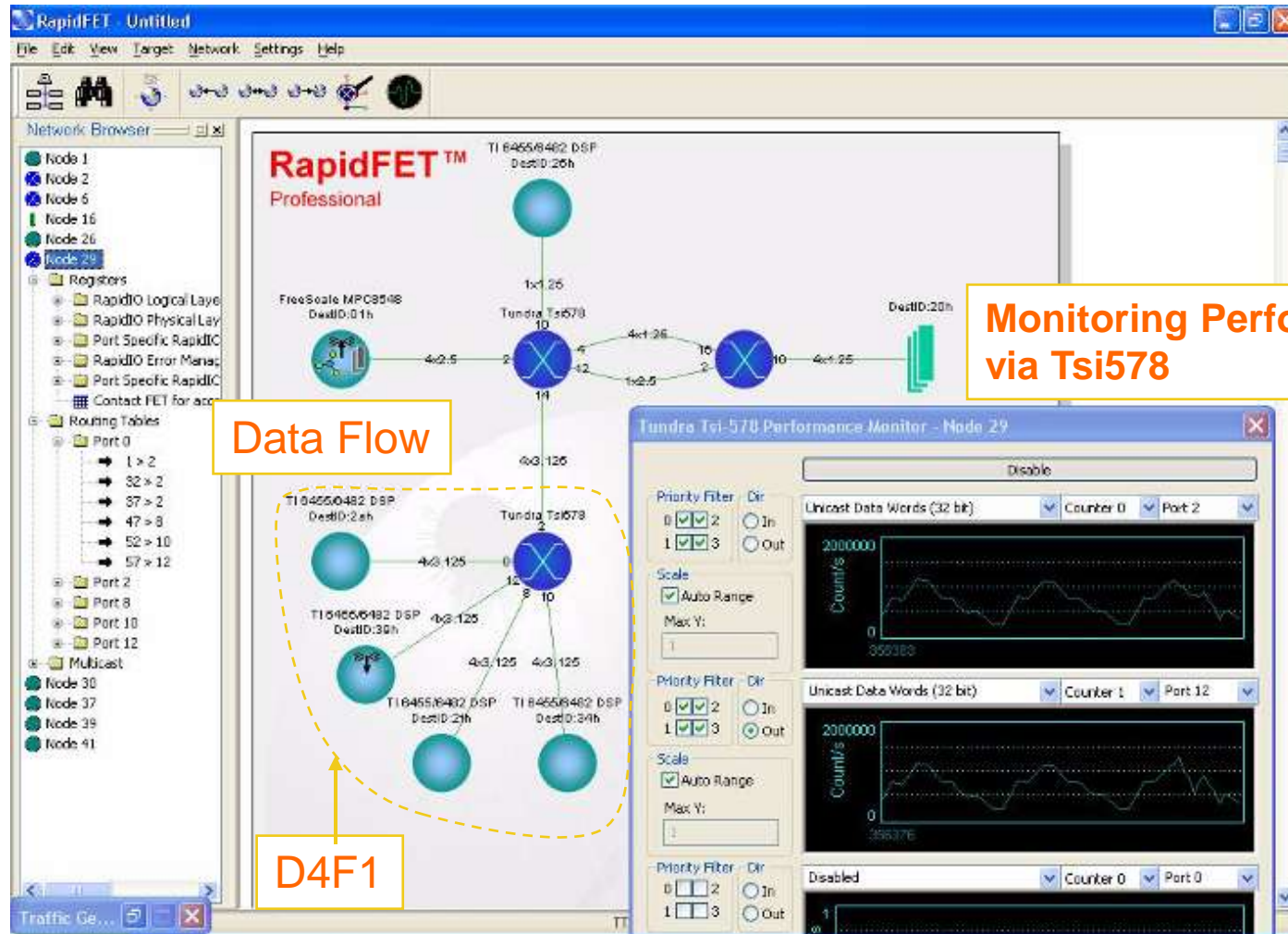
Connect to RapidIO in Backplane via AMC connector

Cost Reduced BB Card with Tsi620 EVB and Commagility AMC 3C87F





- Working example of Serial RapidIO fabric in MicroTCA
 - MicroTCA chassis containing CommAgility AMC-6487C and Tundra Tsi578 MicroTCA Switching Module
 - DSP master RapidIO Enumeration and Management
 - DSP and FPGA endpoint DirectIO data transfer
 - RapidFET graphical RapidIO analysis software
 - Tundra Serial RapidIO Signal Analyzer



The screenshot displays the RapidFET Professional interface. On the left is a 'Network Browser' tree showing nodes and routing tables. The main area shows a network diagram with nodes like 'TI 6455/6462 DSP' and 'FreeScale MPC8548'. A yellow dashed box highlights a specific network segment labeled 'D4F1'. On the right, a 'Tundra Tsi-578 Performance Monitor' window shows two graphs of 'Unicast Data Words (32 bit)' with 'Counts' on the y-axis.

Data Flow

Monitoring Performance via Tsi578

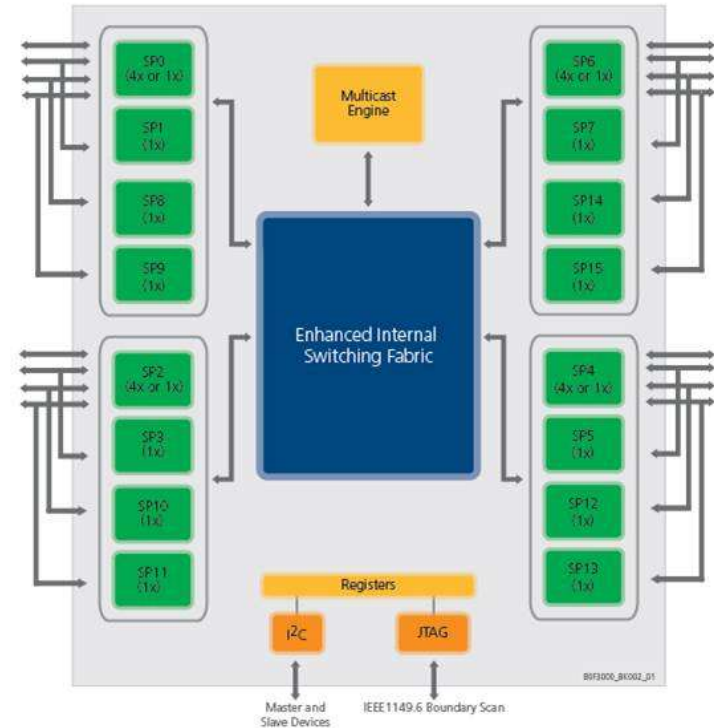
D4F1



Wireless Systems Cost Reduction
and Performance Enhancement with
Tundra Tsi577 and Tsi620



- 40Gbps Full-Duplex Serial RapidIO Switch
- Open Standard Compliant
 - RapidIO Interconnect Specification (Revision 1.3) Compliant
 - 1149.6 AC-JTAG
- Configurability
 - **Up to Sixteen x1 links four x4**
 - Multicast Event Control Symbol
 - Lane Swap
- Performance
 - Cut-through latency ~110ns
 - Multicast
- Low Power
 - **10% power reduction from existing Tsi57x architecture**
 - Programmable SerDes
 - Port Power Down
- Cost
 - **Small 21x21mm HSBGA**
 - Integrated XAUI SerDes
- Availability
 - Sampling Now

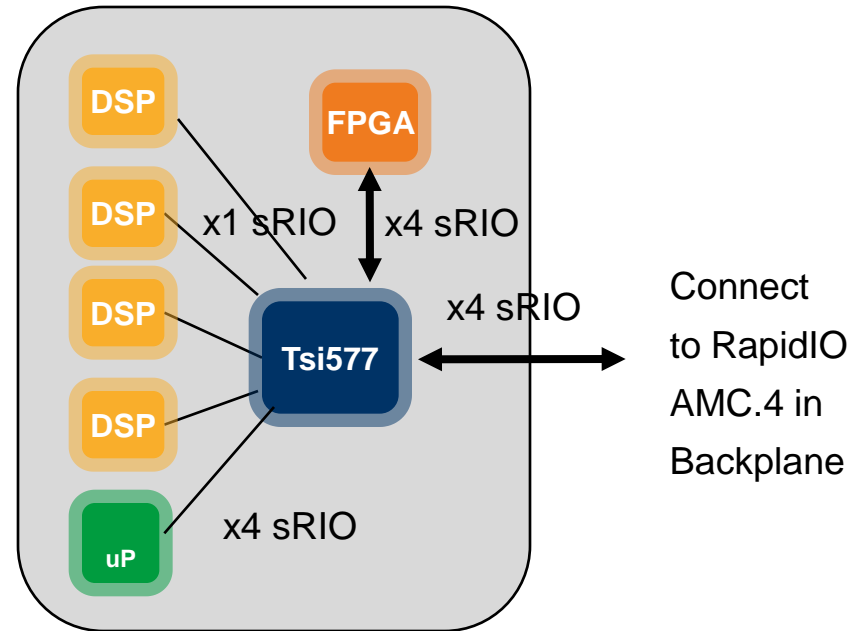


Announced on Oct 23rd

- Small Form Factor ideal for uTCA
- Cost Comparable to PCIe and GbE
- Lowest latency and Power,
- 10% reduction vs existing Tundra switches

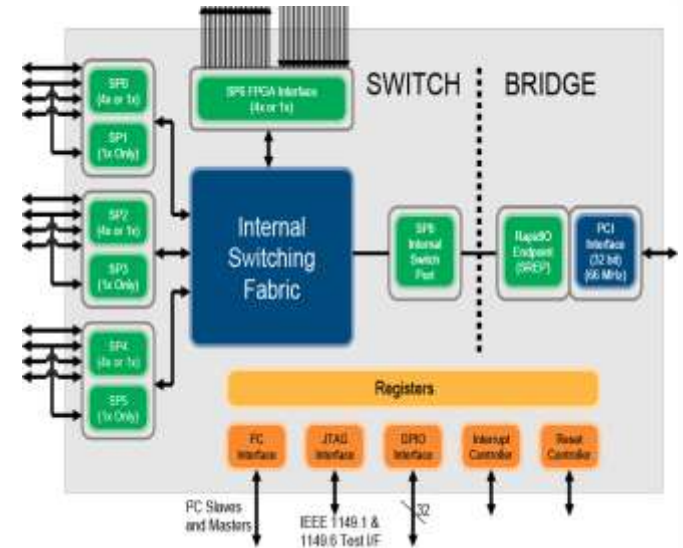
- Three x4 RapidIO links used for :
 - FPGA (OFDMA Phy Processing and Turbo Decode offload) ,
 - microprocessor and
 - for backplane
- Four RapidIO x1 used for DSP cluster
- Optional microprocessor may be on card or on separate processor/host AMC. Microprocessor also used for MAC layer processing
- Antenna data terminated in FPGA for OFDM processing

WiMAX/LTE AMC's

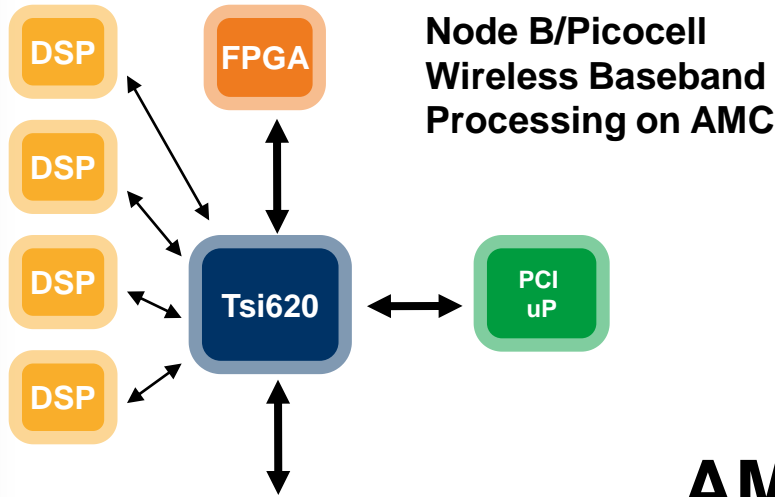


Tsi577's small form factor ideal for Processor Aggregation on AMC.4 spec

Interface	Benefits
Bridging from RapidIO to PCI	<ul style="list-style-type: none"> • PCI V2.2 Compliant 32/66 • Allows direct access to PCI-enabled processors for lower system cost • Leverage reuse of existing software for fast time to market and low risk • Access to investment in existing ASICs seamlessly
Serial RapidIO V1.3 Compliant Switch	<ul style="list-style-type: none"> • RapidIO 1.3 Compliant • Allows 3x the processing power in same form factor as existing solutions, leveraging RapidIO interface to multi core DSPs • Local DSP aggregation using low cost embedded RapidIO switch with proven interoperability with TCI6482, TCI6487, TCI8488 and TCI6484 using line rates from 1.25 Gbaud to 3.125 Gbaud with 3x4 or 6x1 port configuration options • Supports non standard speeds like CPRI and OBSAI reducing cost associated with multiple clocks • Low power per serial port (120-200mW) optimizing system power consumption
FPGA Interface	<ul style="list-style-type: none"> • Connect via RapidIO without cost of embedded SerDes from 1 Gbps to 10 Gbps data rate • Interface to non SerDes FPGA using RapidIO protocol over XGMII physical layer, reducing costs • Option to go to hardcopy to further reduce system cost

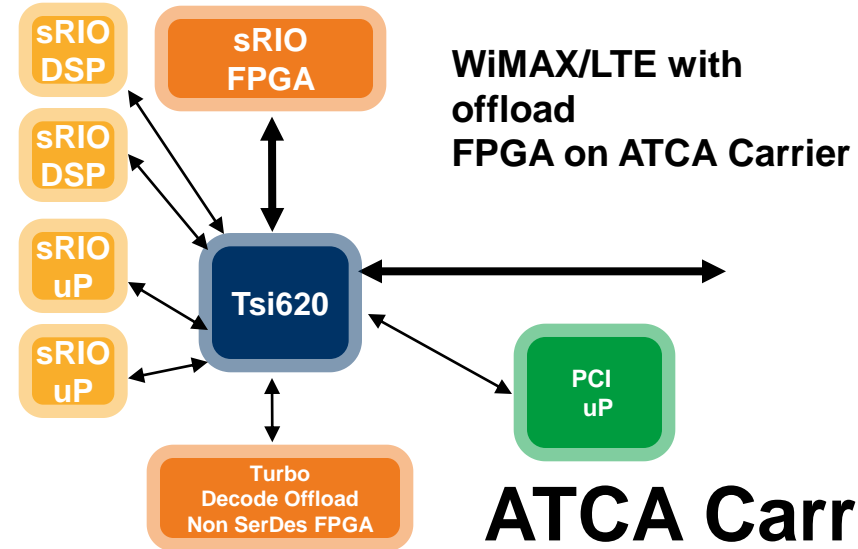


Baseband: 3x processing capacity with BOM cost savings ~\$100



AMC

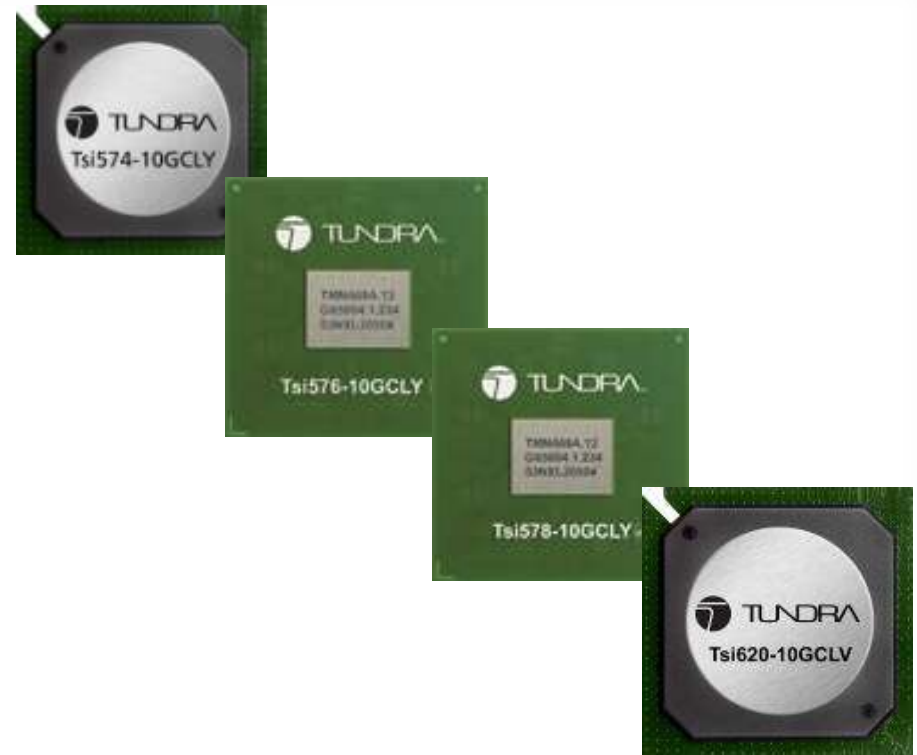
- RapidIO to PCI bridging in hardware for low cost microprocessor
- DSP aggregation: TCI6482/8484/8487/6488, MSC8144 using sRIO ports
- Interface to low cost FPGA for both OFDMA and turbo decode offload
- X4 sRIO to backplane
- Could be “dual width”



ATCA Carrier

- RapidIO to PCI bridging in hardware to low cost host processor
- Optional RapidIO Microprocessor for MAC layer processing
- Dual FPGA solution with no SerDes FPGA for OFDMA/Turbo decode
- SerDes enabled FPGA for CPRI termination
- X4 sRIO to backplane
- DSP aggregation: TCI6482/8484/8487/6488, MSC8144

- **Tsi578™**: Eight x4 links or sixteen x1 links or combinations of x4 and x1
- **Tsi577™**: Sixteen x1 links or four x4
- **Tsi576™**: Twelve x1 links or two x4 and eight x1 links
- **Tsi574™**: Four x4 links or eight x1 links or combinations of x4 and x1
- **Tsi572™**: Eight x1 links or two x4 and four x1 links



9 of Top 10 Wireless OEMs

**Wireless vendors using
Tundra RapidIO Switches today**

**Lowest Power, Multicast, Advanced
Traffic Mgmt, Performance
Monitoring, RapidIO 1.3 Compliant
Family**



Thank You

