
GDA's Participation in RapidIO Eco-system

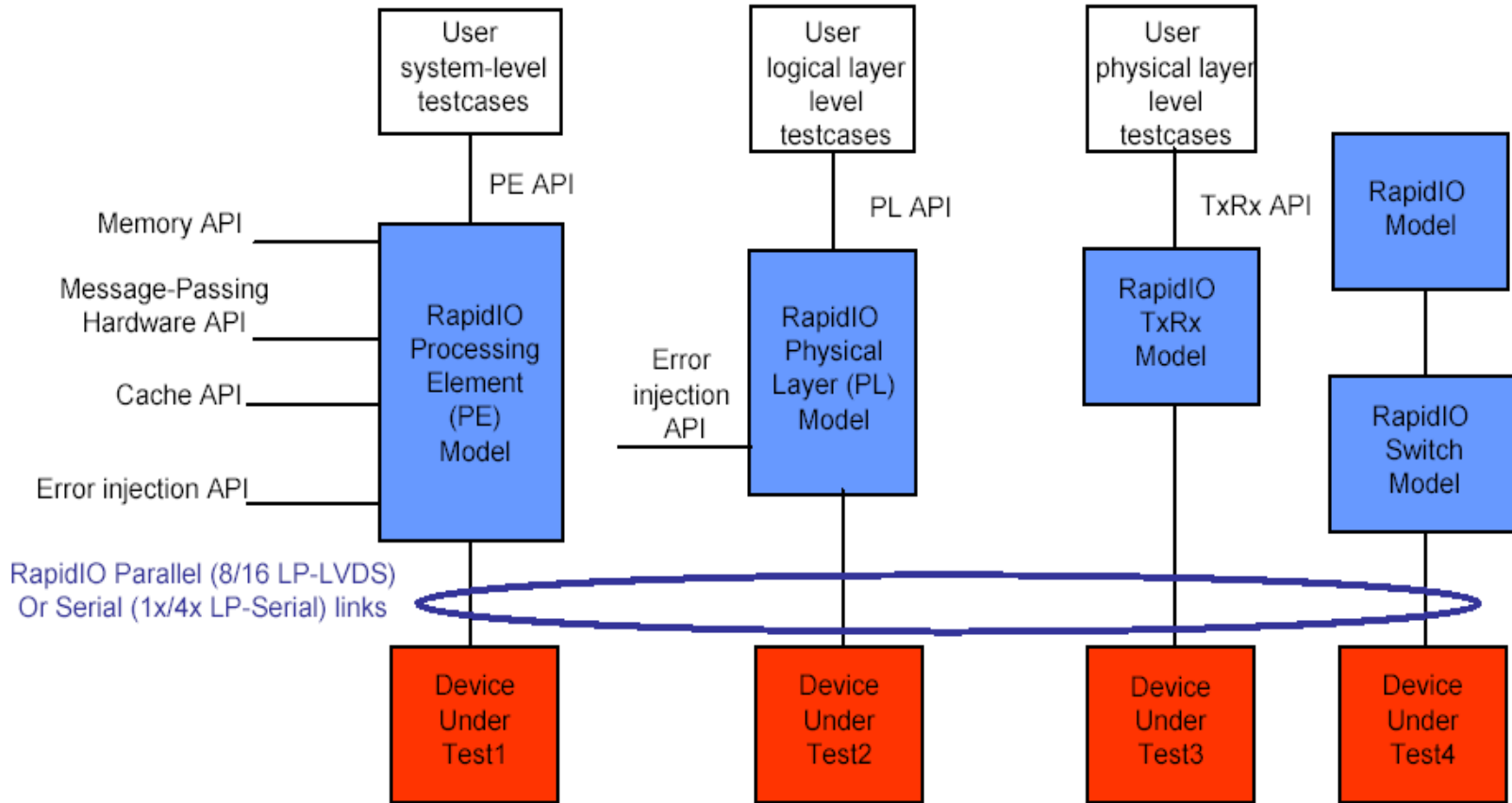


GDA Technologies, Inc.

GDA'S ROLE IN RIO TA BFM

- Bug fixing (Maintenance and Support)
- Enhancement of RIOBFM from 1.2 to 1.3 version
- Subsequent upgradation of RIOBFM from 1.3 to 2.0 version.

RIO TA BFM



RIO TA BFM

- Serial and Parallel RapidIO models compliant to RapidIO 1.3 specification
- Being upgraded to RIO 2.0
- Various levels of test case abstraction provided (symbol, packet, transaction levels)
- Support block, chip, system level verification
- Error injection capabilities
- Error detection and reporting on the interface
- Easy to integrate through flexible C API
- Offers significant interoperability value

RIO TA BFM

Feature & Timelines

- RIOBFM 1.3 Features – Completed 2006
- 1.3 Bus Checker – Q3, 2007
- RIOBFM 2.0 – 4 Phases
 - Phase1 Features – completed -- Q2 2007
 - Phase 2 Accelerated Features – completed – Q2 2008
 - Phase2 Features – ongoing, Q3 2008
 - Phase3 Accelerated Features – completed – Q2 2008
 - Phase 3 Features – to be completed by Q1 2009
 - Phase4 – Maintenance mode

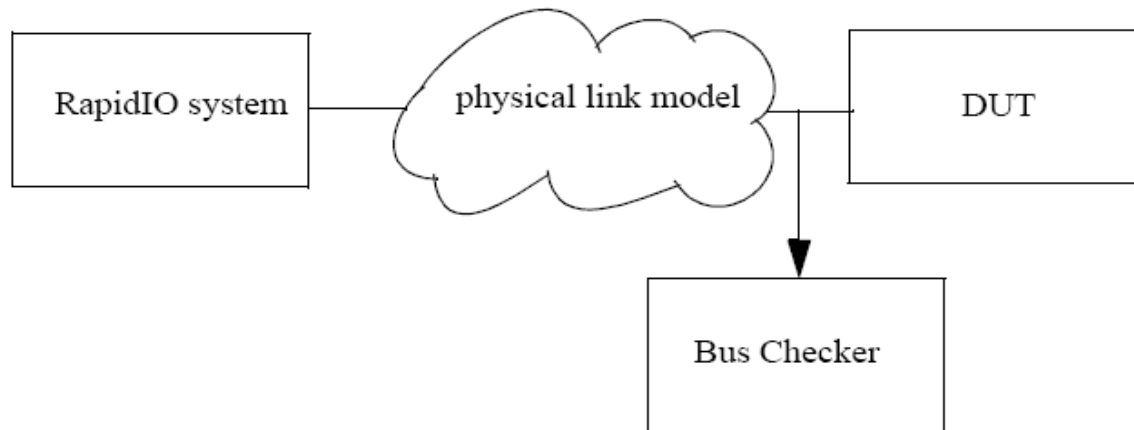
RIOBFM 1.3 Features

- Increased payload size from 32dwords to 64dwords
- Logical Layer Flow Control – Ftype 7 Support
- Data Streaming - Ftype 9 Support
- Inclusion of new transaction type (ttype C & E) for write class packets
- Auto port width detection
- Extended mailbox support
- Enhanced error injection capabilities
- Support for 10 bit interface



1.3 Bus Checker

- Independent component, for checking the DUT behaviour
- Violation in the protocol on the link would be reported



1.3 Bus Checker Features

- Logical Layer Flow Control – Ftype 7 Support
- Data Streaming - Ftype 9 Support
- New transaction type (ttype C & E) for write class packets

SRIO 2.0 – 4 Phases

- Phase1 - **Early access** - Supports minimum functionalities, with which people can test upto link initialization, exchanging RIO2.0 long control symbols
- Phase2 - **Full Function** - Supports bulk of PHY functions...testing with this, people can take their code to FPGA with low level PHY settings. Basic error injection capabilities are also included
- Phase 2 – **Accelerated Features** – Support for x2 link width, Scrambler/Descrambler, Virtual Channels, Reliable/Continuous Traffic mode, Error Injection
- Phase 3 – **Accelerated Features** – Support for Transmit Preemphasis/Adaptive Equalization, Baud Rate Selection, Multicast Symbol
- Phase3 - **Final Support** - Advanced/Optional features left out in Phase2, corner cases, Enhanced error injection capabilities
- Phase4 – **Maintenance** and bug fixing



RIOBFM 2.0 Phase1 Features

- Long Control Symbol
- IDLE2 sequence without scrambler.
- Supported link widths : 1x and 4x



RIOBFM 2.0 Phase2 Features

- Scrambler/Descrambler Implementation
- New link widths (2x, 8x & 16x)
- Support for RIO2.0 LP-Serial CAR/CSR register set
- Link compliance checking enhancements in addition to existing RIO1.3 checks
- Basic Error Injection capabilities
- Column-Padding error checks



RIOBFM PHASE2 ACCELERATED FEATURES

- Support for x2 link width
- Long Control Symbol implementation of 2x mode.
- Virtual Channel implementation upto 9VC's.
- Error injection capabilities
- Support for Reliable/Continuous Traffic modes.
- Check the frequency of status/vc status control symbols.

RIOBFM 2.0 Phase3 Features

- Enhancement of Data Streaming - Reliable traffic/Continuous traffic VC (Virtual Channel) support
- Enhancement of Flow Control
- Enhancement of Multicast
- Support for optional Baud rate detection/selection
- Support for automated RX Equalization training in IDLE2
- Support for TX Pre-emphasis control by RX
- Enhanced Error-Injection capabilities
- Support for port width override functions



RIOBFM 2.0 PHASE 3 ACCELERATED FEATURES

- Multicast Symbol
- IDLE2 automated RX equalization training
- IDLE2 TX preemphasis control by RX
- Baud Rate Selection
- Port Width Override function

GRIO: First complete RapidIO IP Solution



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Press Release

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GDA Technologies Announces GRIO--Silicon IP Cores Based on Serial and Parallel RapidIO® Technology

GDA Joins the RapidIO Trade Association

San Jose, California – April 26, 2004 - GDA Technologies, Inc., a fast growing supplier of Silicon Intellectual Property (SIP) and Electronic Design Services (EDS), today announced the availability of GRIO (GDA RapidIO controller IP cores). GRIO IP cores are fully compliant with the Serial and Parallel RapidIO specifications and are targeted for embedded, communications and networking applications. The GRIO solution is derived from the RapidIO technology-based controller design licensed from Freescale Semiconductor, a wholly owned subsidiary of Motorola Inc.

GRIO IP is packaged as a highly configurable, reusable design and marketed worldwide by GDA as the GRIO RapidIO IP family. GDA also announced today that it has joined the RapidIO Trade Association and will become an active member of the association in accelerating its global deployment.

"RapidIO interconnect architecture provides best-in-class features in performance, scalability and reliability, which are fundamental requirements for connectivity in high-speed applications. Our GRIO IP cores provide a set of features and capabilities that will



GRIO: RapidIO Controller



PRODUCT BRIEF

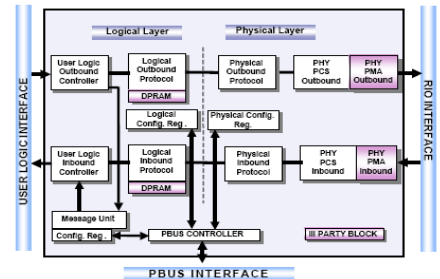
**High Performance
 Technology Independent
 System Validated**

- Compliant with RapidIO specification, Revision 1.2
- Supports both Serial and Parallel interfaces
- Supports 1x and 4x serial interfaces at 1.25/2.5/3.125Gbps
- Supports 8 and 16 bit parallel interfaces at 250/375/500 MHz
- Implements physical, transport and logical layer functions
- Supports both input/output and message passing protocols
- Implements receiver controlled flow control
- Supports all transaction flows and priorities
- Support for up to 256 bytes data payload
- Supports 34 bit addressing
- Implements a flexible buffer management scheme
- Performs link initialization, training, error detection and recovery
- Performs auto detection of interface widths and modes
- Supports multi-cast event control symbols
- Targets FPGA, Structured ASIC and Standard Cell technologies

The RapidIO Interconnect Architecture, designed to be compatible with the most popular integrated communications processors, host processors, and networking digital signal processors, is a high-performance, packet-switched, interconnect technology. It addresses the high-performance embedded industry's need for reliability, increased bandwidth, and faster bus speeds in an intra-system interconnect. The RapidIO interconnect allows chip-to-chip and board-to-board communications at performance levels scaling to ten Gigabits per second and beyond.

GDA's RapidIO controller core (GRIO) is designed to meet the growing needs of the industry. The core's simple, configurable and layered architecture is independent of applications, PHY designs, implementation tools and, most importantly, the target technology. The hardware and software configurable features make the core suitable for use in multiple applications. The design targets embedded systems, telecommunication, networking and any application where high speed, low latency response, low pin counts, reliability and scalability are necessary.

GDA's RapidIO Controller solution leverages years of experience in PCI, PCI-X, HyperTransport and PCI Express technologies and the expertise in creating fully compliant, system validated, interoperable IP solutions with RTL, synthesis, simulation, board and software components. GDA is the leading solution provider for fast interconnect technologies like HyperTransport, PCI Express and 10G Ethernet with many licenses sold in the compute and networking markets.



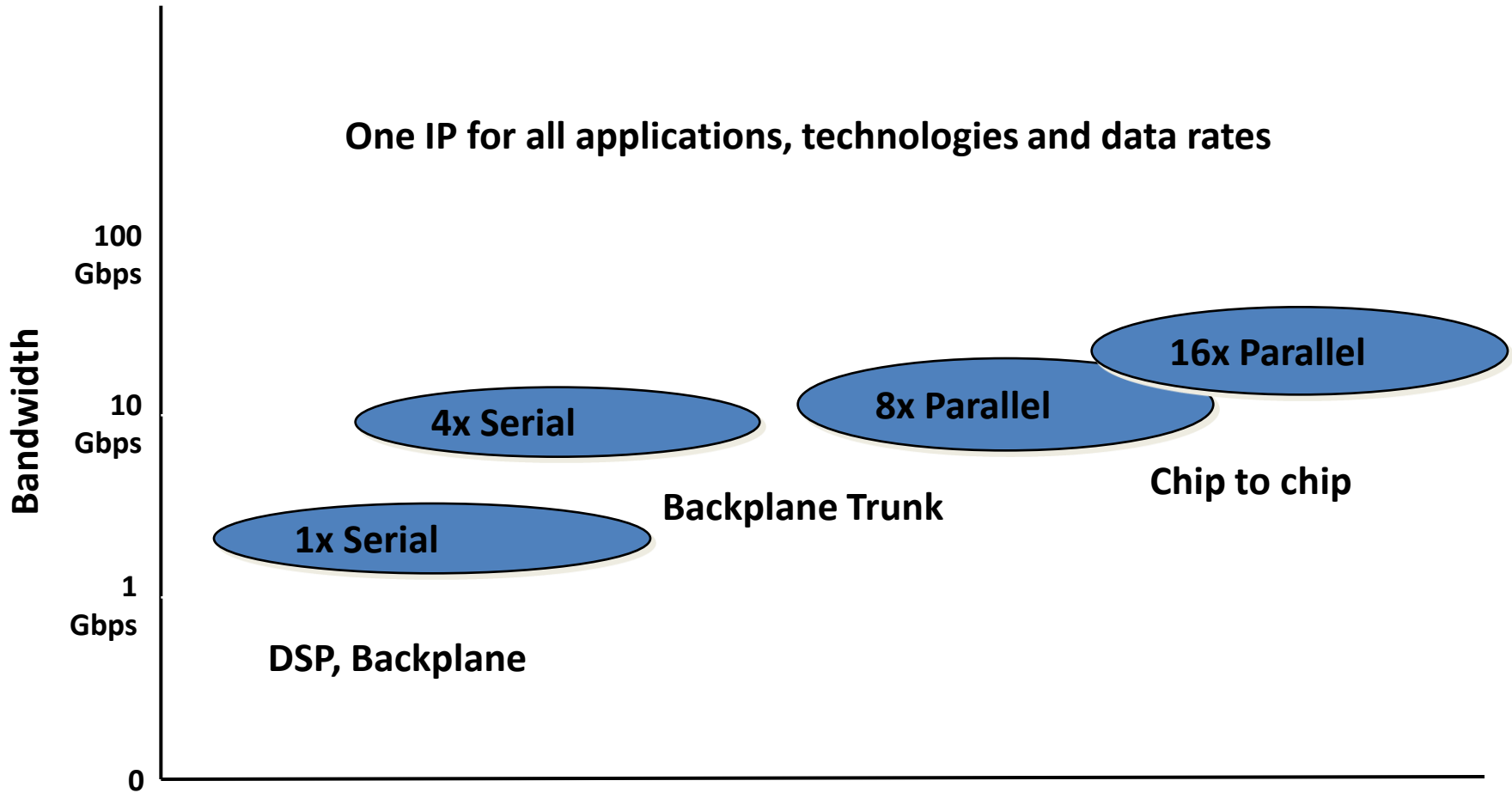
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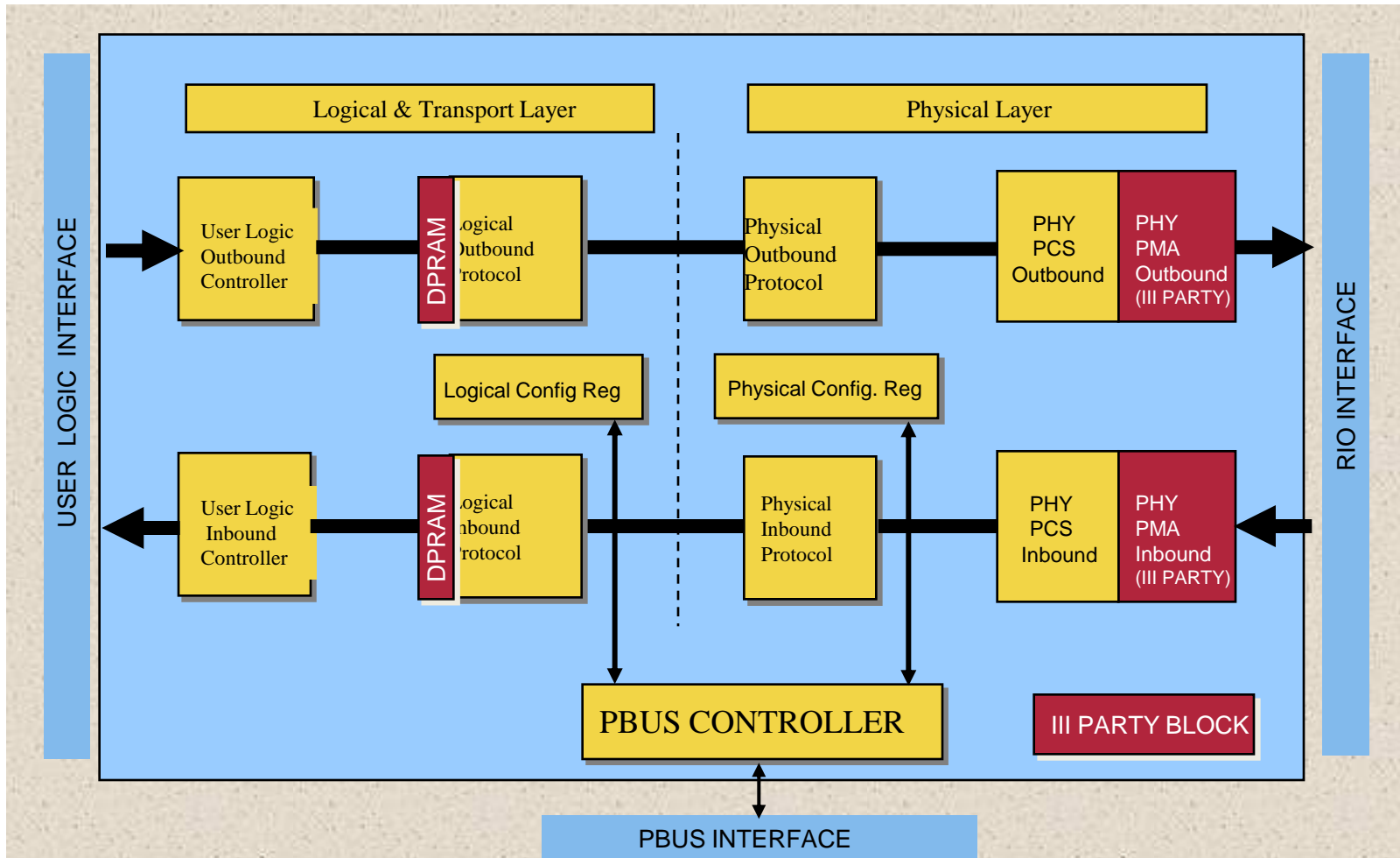
GDA Technologies, Inc.



Highly configurable IP



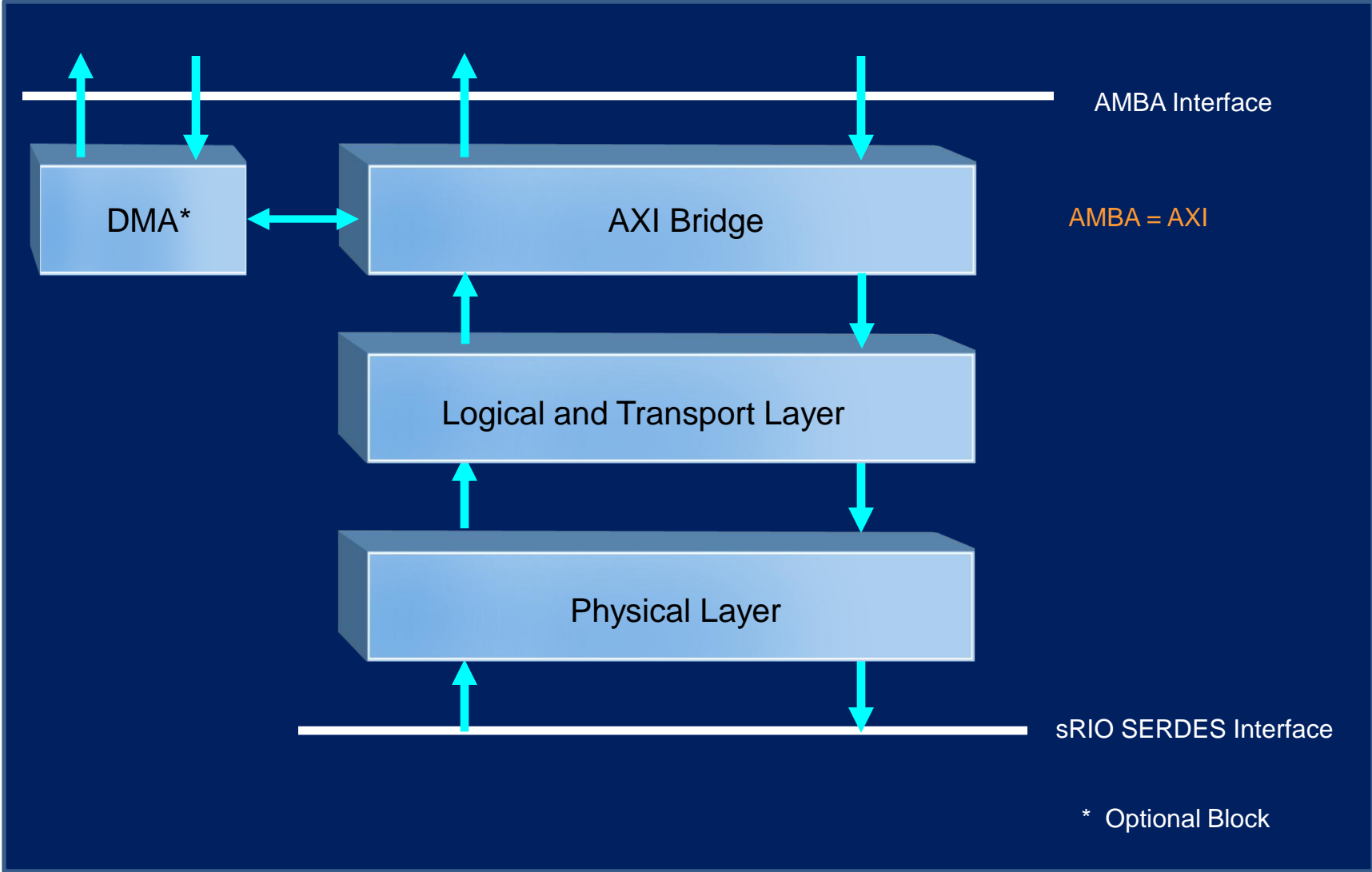
GRIO Architecture



GRIO Features

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RapidIO to AXI Bridge (RAB)



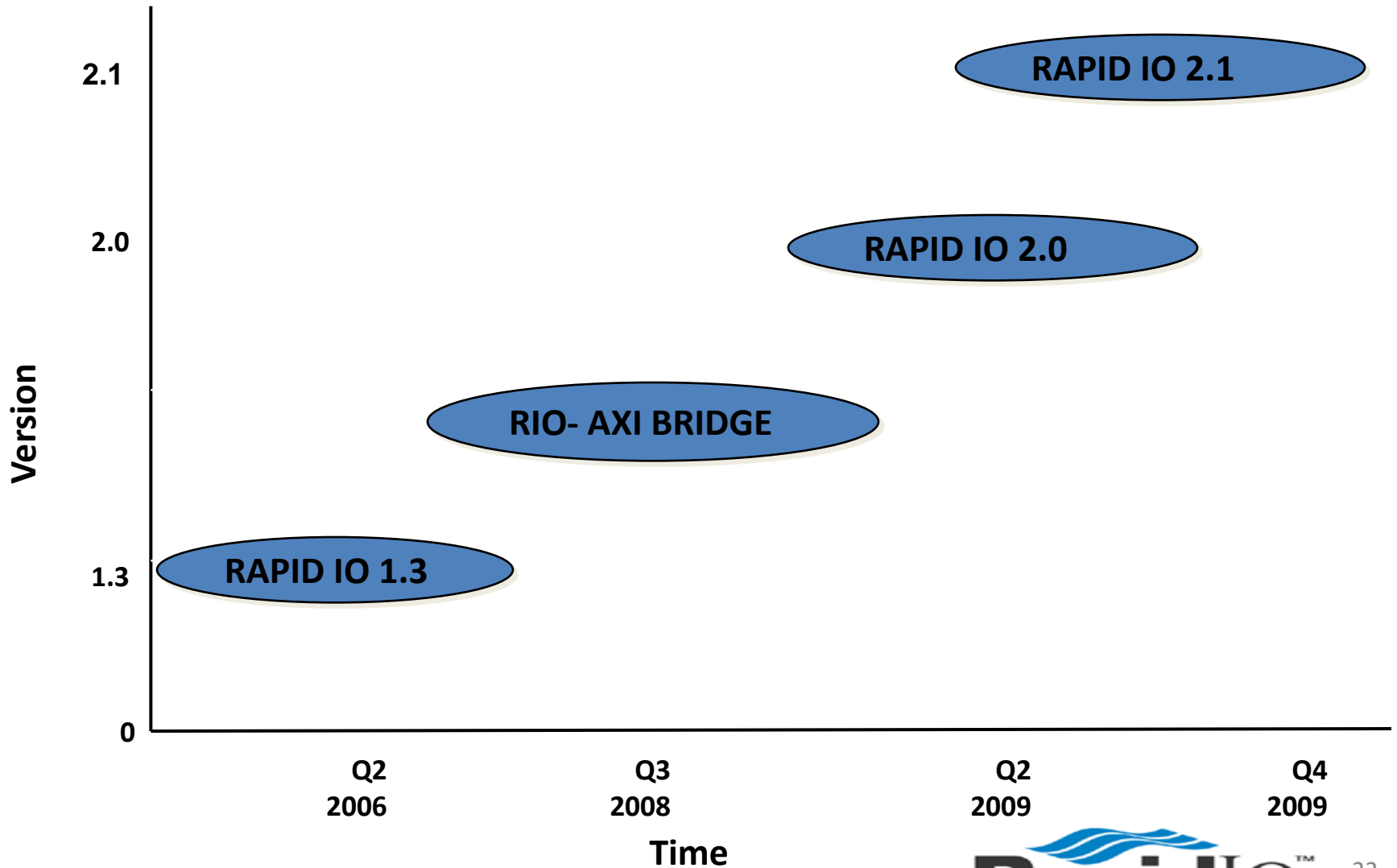
AXI Bridge Features

- Compliant to AMBA AXI protocol v1.0
- Supports 32-bit or 38-bit addressing
- Provides AXI PIO operation support
- Provides RIO PIO operation support
 - Configurable number (1-8) of RIO PIO Master
 - Configurable number of pending request
- Mailbox and Doorbell Support
 - Configurable number of Outbound Letters
 - Configurable number of Inbound Letters
- Write and Read DMA
 - Configurable number of Write DMA
 - Configurable number of Read DMA
 - Configurable DMA type - Descriptor based or Register based
 - Configurable arbitration schemes between DMA and PIO transactions - Round Robin or Strict Priority

RAB Features

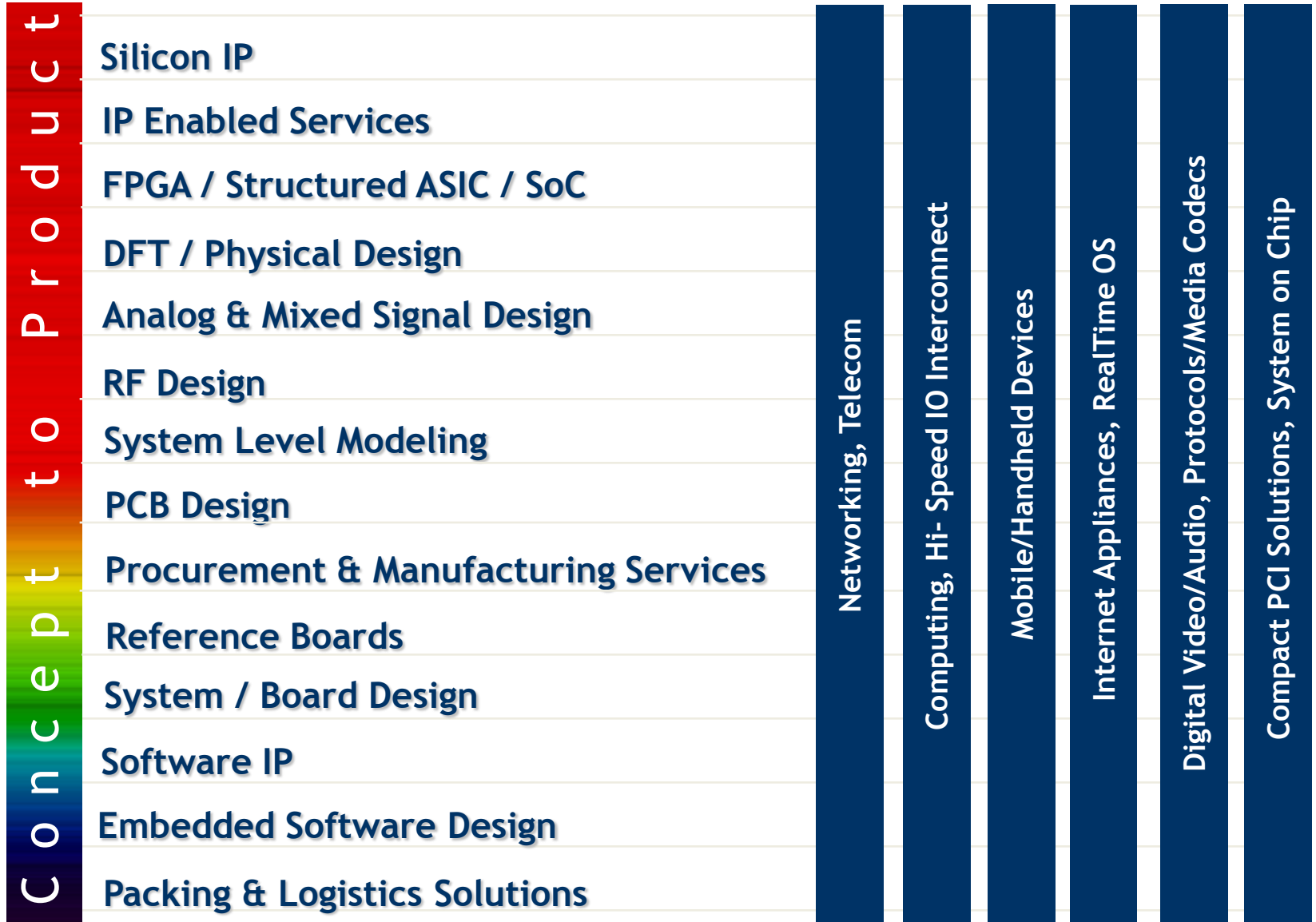
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GDA RapidIO IP Roadmap



GDA DESIGN SERVICES

APPLICATIONS



For More Information on GDA RIO Program:

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