

# Overview and Spec Gen2 Features and Spec. Changes comparisons

*RapidIO Global Design Summit*

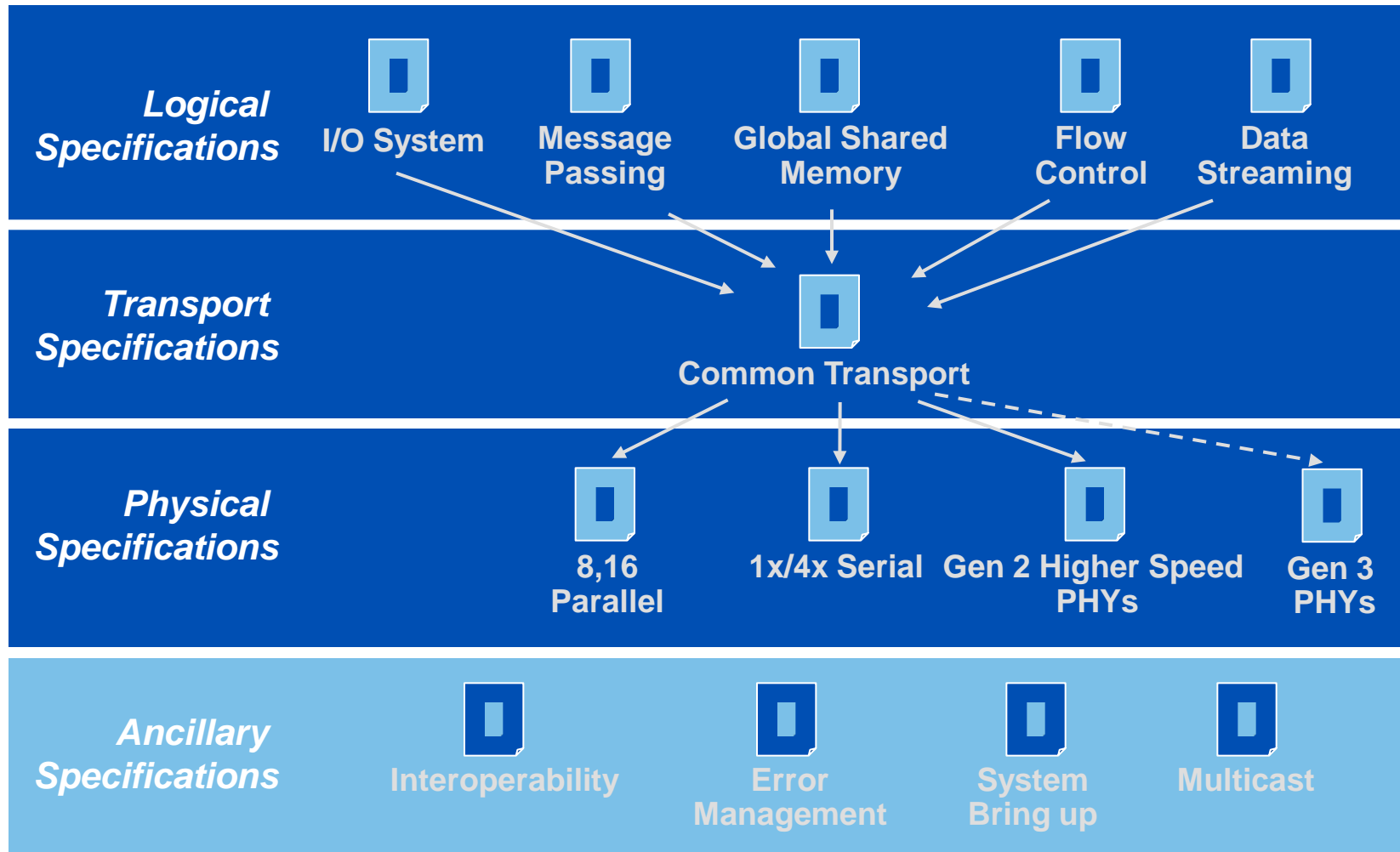
*Tom Cox*

*RapidIO Executive Director*

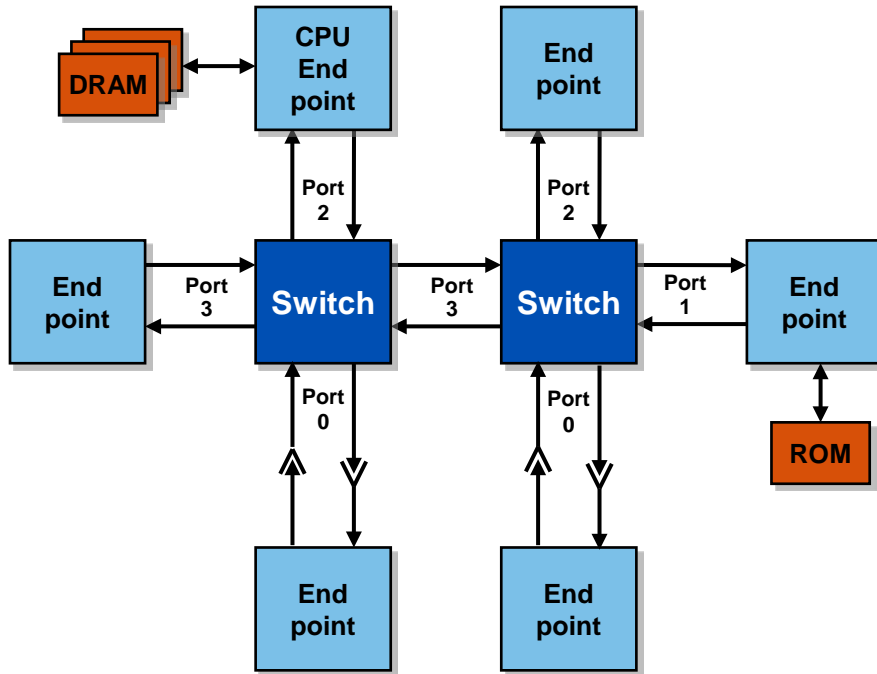


The Embedded Fabric Choice

# RapidIO Architecture



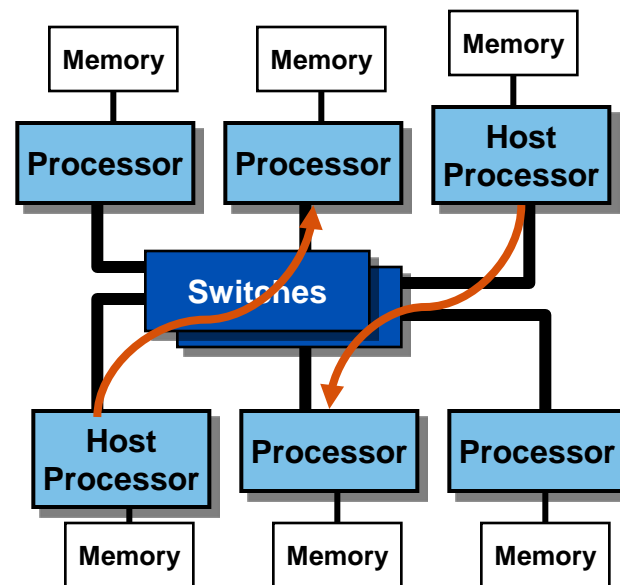
# RapidIO Network Building Blocks



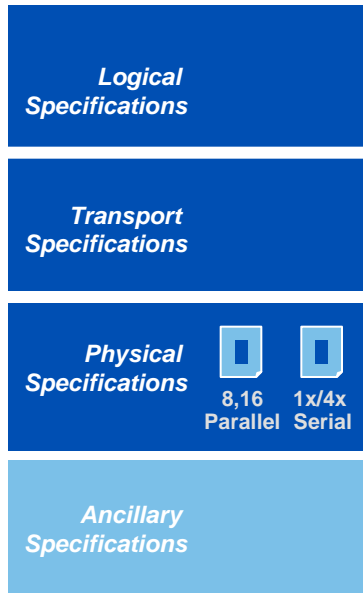
- RapidIO networks are built around two “Basic Blocks”
  - Endpoints
  - Switches
- End points source and sink packets
- Switches pass packets between ports without interpreting them
- All devices support maintenance transactions for access to configuration registers

# RapidIO Technology System Value

- Scalable, modular architecture
  - Layered architecture with common transport layer
  - Chip-to-chip, board-to-board, backplane
- High-speed connectivity
  - Physical layer defined for backplane interconnection
    - ~80-100 cm + 2 connectors (Serial)
  - Up to 10Gbps bandwidth today
- Robust feature set
  - Carrier-grade reliability
  - Traffic management
  - Multi-protocol/convergence

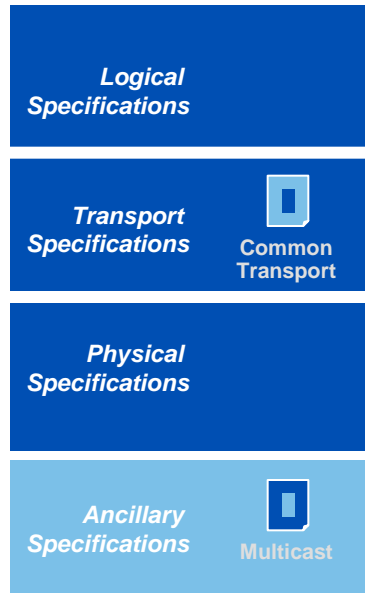


# Physical Layer Specifications



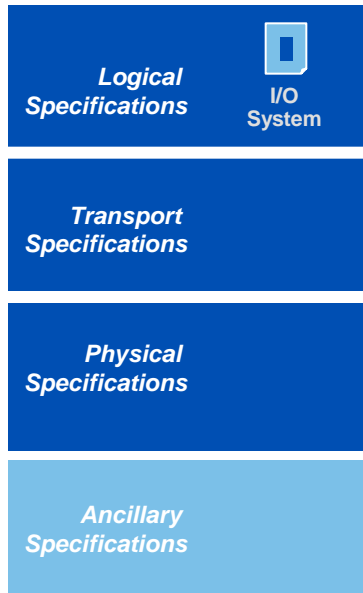
- Serial
  - 1 or 4 lane XAUI AC coupled with 8/10b encoded
  - 1.25 - 3.125 Gbaud aggregated up to 10Gbps
- Parallel
- Point-to-point topology
- Device synchronization and training
- Control symbols provide for physical layer control
  - Pre-empt data packets
  - Explicit hardware-based error recovery using retransmission protocol
- Four fixed priorities
  - Mechanism for higher and lower priority traffic
  - Order is maintained for traffic at a given priority
  - Transaction acknowledge/reply higher priority than request
- Link-level flow control

# Transport Specification



- Switches operate at the transport layer
  - All logical protocols use a common transport header
  - Today's switches will work with future logical protocols
- Device-based routing
  - 8 or 16 bit device ID
    - Simplifies classification and routing compared to Ethernet or IP
  - Any RapidIO device ID can be used as a unicast ID or a multicast group
    - Unicast packets are forwarded out a single port
    - Multicast packets are forwarded to multiple ports (No ACK NWRITE, SWRITE, Data Streaming)
  - Fail-over events only affect routing table entries of nearest neighbors

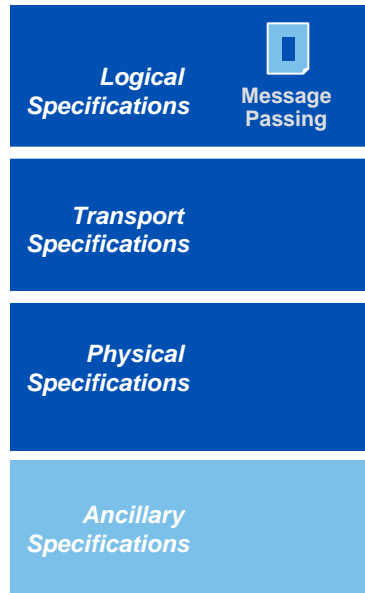
# Input/Output Logical Specification



- Load / Store / DMA operations
  - Processor is not necessarily RapidIO aware
- 34, 50, 66-bit address space
- Transactions:
  - NREAD – read operation
    - Data returned is the response
  - NWRITE – write operation, no response
  - NWRITE\_R – robust write with response from the target end-point
  - SWRITE – streaming write
  - ATOMIC – atomic read-modify-write
  - MAINTENANCE – system discovery, exploration, initialization, configuration and maintenance operations

# Logical Specification

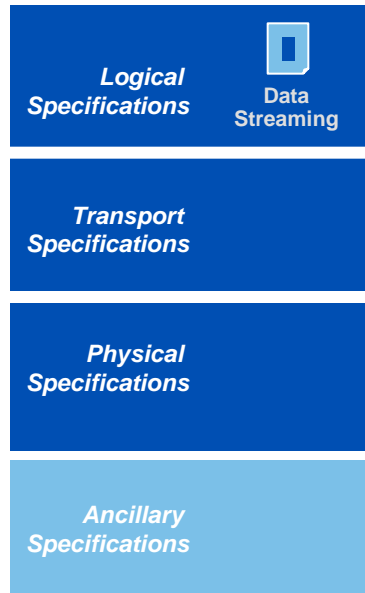
## Message Passing



- Hardware support for segmentation and reassembly of 4kB datagrams
  - Segments are automatically reordered
- Logical Layer acknowledge
  - Auto retry on timeout
- Messages
  - Organized into 4 mailboxes and 4 letters within each mailbox
    - Sending device can send 4 concurrent letters to each target mailbox
- Doorbells
  - Short 8 or 16-bit messages

# Logical Specification

## Data Streaming



- Segmentation and reassembly
  - 64Kb PDUs
  - System-wide MTU size
- Efficient logical protocol for communications
  - Start, continuation, end segments
    - continuation has 20 bit header
- Interworking
  - Ethernet, UTOPIA, SPI-3/4, CSIX, etc
- Virtual Streams
  - Flow identification
- Traffic Management framework
  - End-to-end Flow control
  - Millions of streams
  - 256 traffic classes
  - Lossy operations
    - No logical layer acknowledge to support traffic managed data plane applications

# Other Features

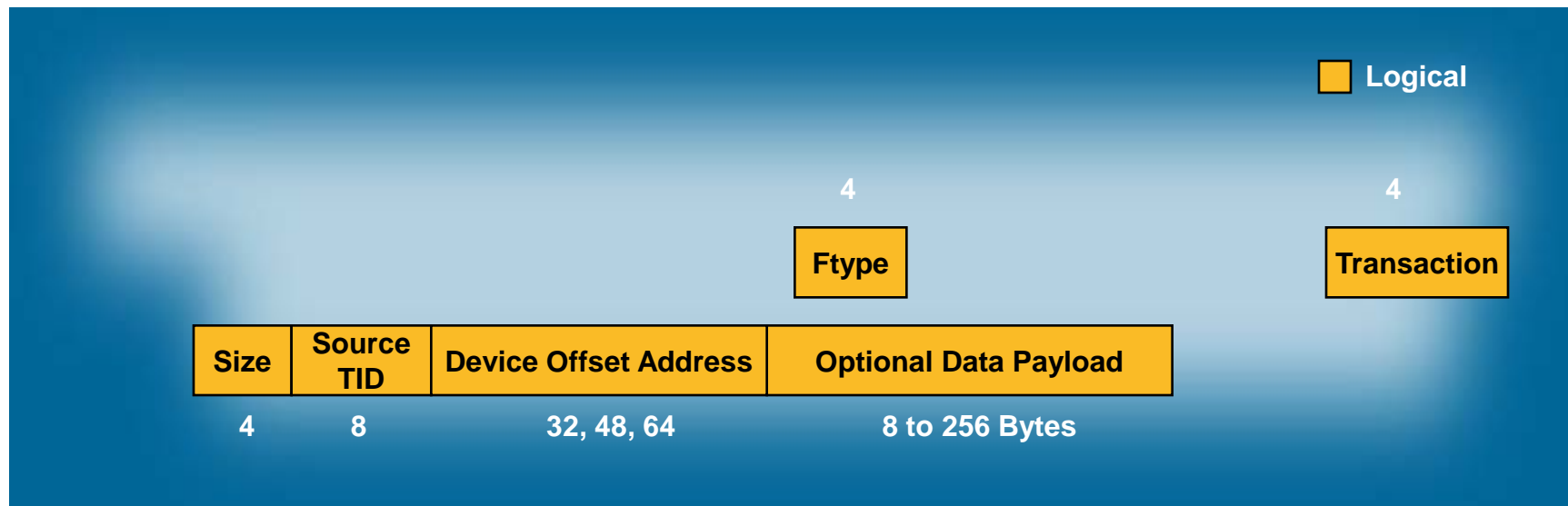
- Specification includes a user-defined logical protocol for custom extensions
- Packets are 256 payload bytes or less
- **Ancillary Specifications**
  - Interoperability
    - PCI transaction mapping
    - Hardware Interoperability Platform (HIP)
    - Interoperability checklist
  - Error Management
  - System Bring-up

# RapidIO Packet Format

## Logical Layer



- Logical Layer format delineated by 4 bit Ftype field Listed as “TYPES” in the Specification
- Transaction field indicates the specific request or response type
- All other fields dependent on Ftype and Transaction



# RapidIO Packet Format

## *Logical TYPES*



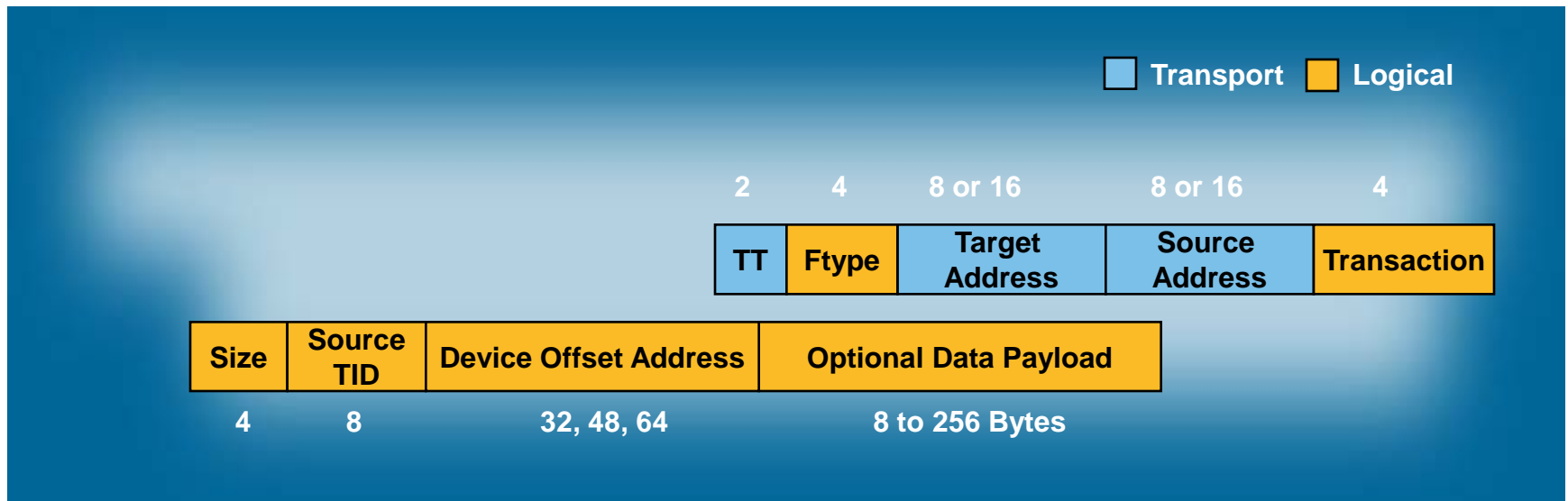
- I/O non-coherent functions
  - NREAD, NWRITE, NWRITE\_R, SWRITE, ATOMIC
- Message functions
  - DOORBELL, MESSAGE
- System support functions
  - MAINTENANCE
- Flow Control
- User Defined functions
- Cache coherence functions
  - READ, READ\_TO\_OWN, CASTOUT, IKILL, DKILL, FLUSH, IO\_READ

# RapidIO Packet Format

## Transport Layer



- RapidIO uses source based addressing
- Switches use route tables to determine destination port
- TT Field indicates size of route address
- A destination may have more than 1 target address for redundant routes

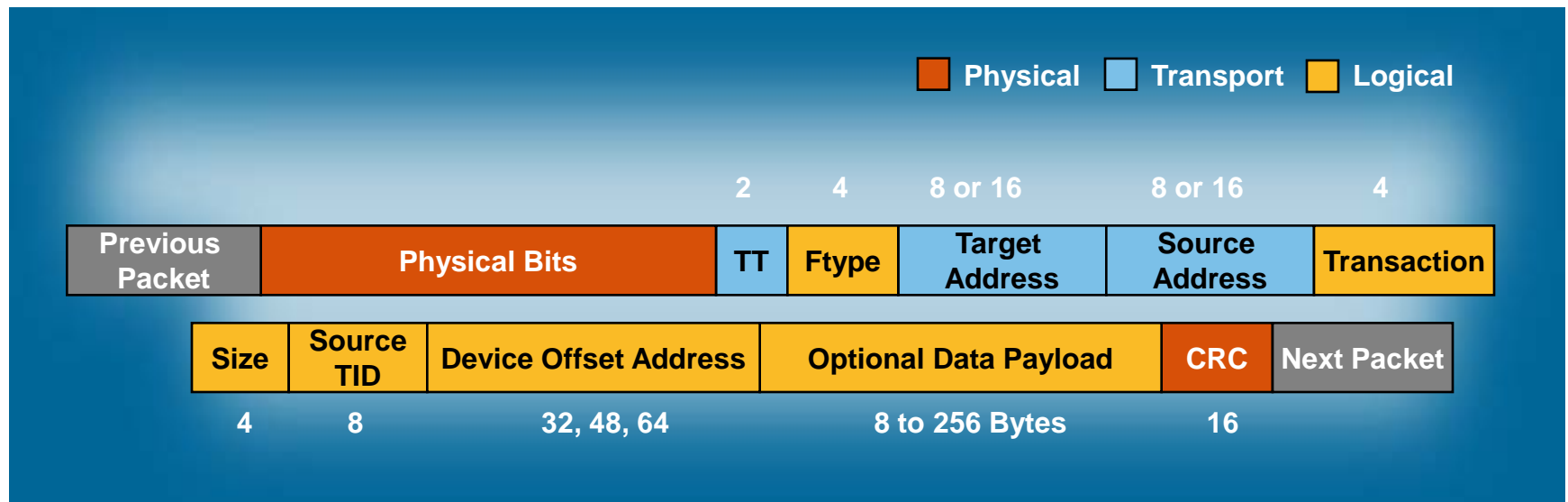


# RapidIO Packet Format

## Physical Layer



- Physical Layer adds device to device handshake info
- Packet partitioned to simplify assembly/disassembly in controllers



# Functional Goals for Data Streaming



- Enhanced Encapsulation Functionality
  - Achieve bandwidth utilization approaching 100%
  - Protocol independence
  - Manage millions of independent streams
  - Support streaming, cut-through architectures
  - Support system-wide MTU size (as low as 32 bytes)
  - Transport 64Kb PDUs
  - Achieve deterministic behavior (including SAR format for fixed packet sizes)
- Semantics for Traffic Managed Fabrics
  - Support hundreds of traffic classes, thousands of flows and fine-grain flow control
  - Implement congestion management and avoidance
  - Provide option to drop traffic when absolutely necessary
- Backwards Compatible
  - Inter-operate with existing RapidIO specifications

# Traffic Streams

- Definition
  - An independent, ordered series of PDUs flowing from a producer to a consumer
- PDUs in a stream...
  - Share the same Tx and Rx device
  - Share an ordering relationship
- PDUs in different streams...
  - Are segregated for differentiated processing or service
  - May have differences in protocol-specific fields
    - Example: UDP port #
- Streams are application defined
- Identified by a unique Virtual Stream ID (VSID)

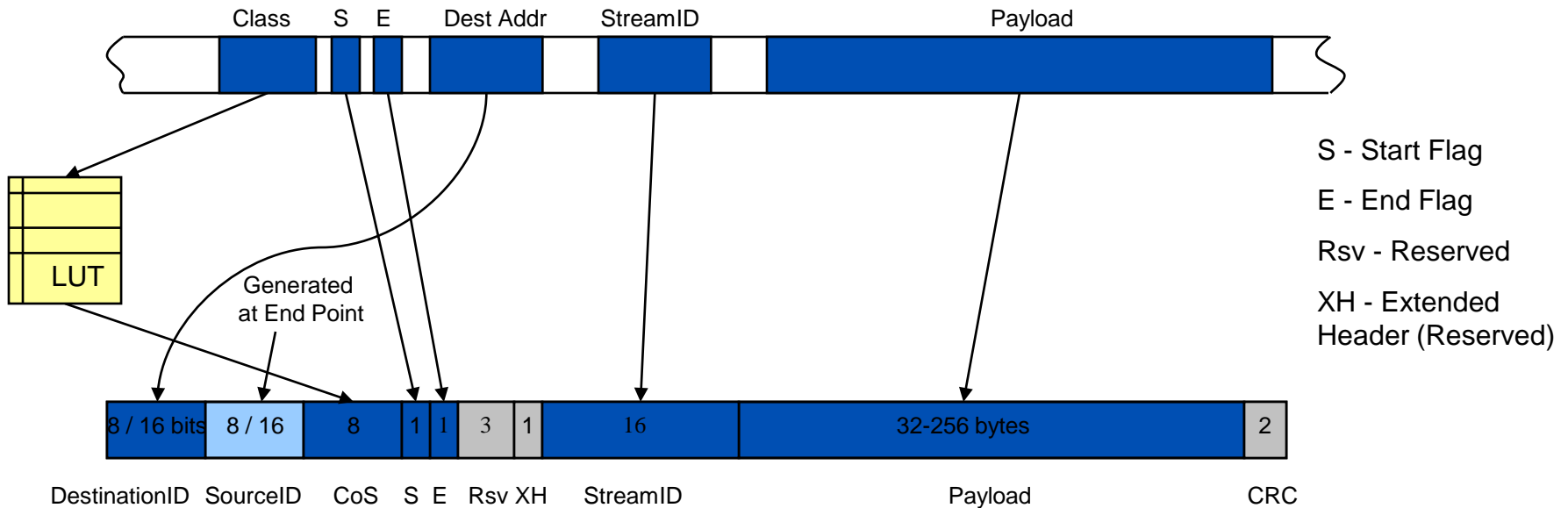
# Virtual Stream ID (VSID)

- Source/Destination pair
- Class of service
- StreamID
  - Can be loaded with any demultiplexing method at the destination
    - Protocol
    - Sub Port Addressing
    - Buffer / Virtual Memory Allocation
  - StreamID is used at the endpoints only
    - *RapidIO end-points terminate traffic*

# Encapsulating Protocols

One possible implementation of encapsulating a **CSIX** frame into a RapidIO Data Streaming PDU

## CSIX Frame (enhanced)

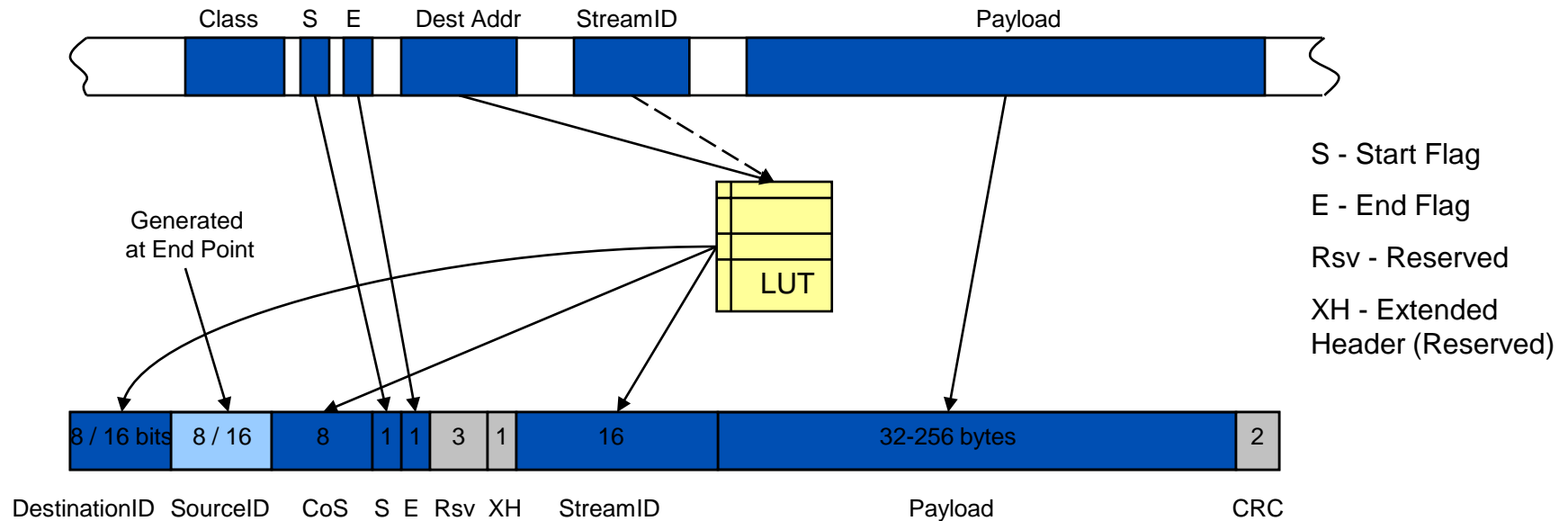


## Rapid IO Data Streaming PDU (start segment)

# Encapsulating Protocols

An alternative implementation of encapsulating a **CSIX** frame into a RapidIO Data Streaming PDU

## CSIX Frame (enhanced)

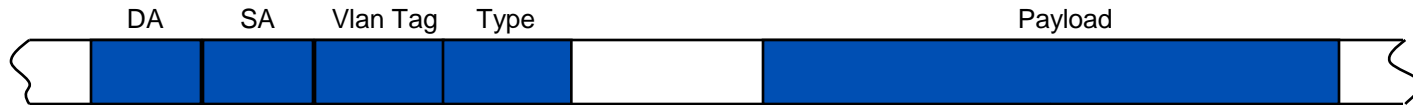


## Rapid IO Data Streaming PDU (start segment)

# Encapsulating Protocols

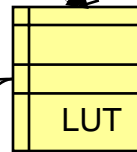
Possible implementation of encapsulating a **Ethernet** frame into a RapidIO Data Streaming PDU

## GMII Frame



Key can be any field(s)

May be broken up to require several PDUs during SAR



Generated at End Point

Generated during SAR

- LUT - Lookup Table
- S - Start Flag
- E - End Flag
- Rsv - Reserved
- XH - Extended Header (Reserved)



DestinationID SourceID CoS S E Rsv XH StreamID Payload CRC

## Rapid IO Data Streaming PDU (start segment)

# Summary

- RapidIO is an **open-standard switched fabric** for wireless infrastructure, edge networking, storage, scientific, military and industrial designs.
- RapidIO delivers the **reliability, cost effectiveness, performance and scalability** required by its target markets.
- RapidIO offers a **broad ecosystem of over 50 partners and suppliers, with products and solutions available for your designs today.**
- *Learn More:* Download the latest RapidIO Specifications
  - **<http://www.rapidio.org/specs/>**



# RapidIO Gen 2

*New Features and Benefits*



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# New Features



- Two major areas of concentration
  - New Higher Performance Physical Layer
    - Next step in bandwidth matching with current SerDes offering
  - Significant Data Plane Enhancements
    - Offering carrier grade Data Fabric Performance

# New Physical Layer Feature Overview



- Rev 2.0 is backwards compatible with Rev 1.3
- Link width options are 1x, 2x, 4x, 8x and 16x
- Signaling rates of 1.25, 2.5, 3.125, 5.0 and 6.25 Gbaud
- Extended channel reach goals and baud rates
- Data is 8b/10b encoded
- Hot plug support at the electrical level
- AC electrical specs
  - Speeds < 3.5 Gbaud are based on 3.125GBaud XAUI
  - Speeds > 3.5 Gbaud are based on OIF
- Introduction of new functionality in control symbol and Idle pattern

# Benefits

- **Backwards compatibility with Rev 1.3**
- Systems will interoperate with existing silicon at speeds lower than 3.5 Gbaud
  - Protects investments made TODAY!
- Provides a flexible solution to system architectures' mix of traffic requirements
- Provides a migration path for backplanes going forward

# Benefits

- Combination of Link width (1x, 2x, 4x, 8x and 16x) and Signaling rates (1.25, 2.5, 3.125, 5.0 and 6.25 Gbaud)
- Scalability: Meets the needs of any possible architecture
  - Backplane application
  - Chassis to chassis
  - Processor interconnect to I/Os and System
  - DSP clusters
  - Bridging/Encapsulation of any other protocol like SPI4, PCIe 1.1 or 2.0, Utopia, GigE and 10 GigE
- Flexibility of architecture in the field
- Protection of the investment (SW and HW) for customers

# Benefits

- Extended Reach and baud rates
- Baud rates of 1.25, 2.5 or 3.125 Gbaud
  - Long Reach: 50 cm channel length with 2 connectors
  - Short Reach: 20 cm channel length with 1 connector
- Baud rates of 5.0 and 6.25 Gbaud
  - Long Reach: 100 cm channel length with 2 connectors
  - Medium Reach: 60 cm channel length with 2 connectors
  - Short Reach: 20 cm channel length with 1 connector
- Support for DFE based receivers offers additional channel choices
- Supports Stateye channel compliance testing
  - Valuable for closed data eye evaluation
- Reliably meets the application needs based on reach
- Adaptable to any part of the system

# Benefits

- Data is 8b/10b encoded
- Packet data will be scrambled for all baud rates > 3.5 Gbaud
- Scrambling occurs after lane stripping and before 8b/10b encoding (one scrambler per lane)
- Provides better EMI suppression and Reliability
- Allows use of special 8b/10b characters for delineation
- Makes use of existing test equipment infrastructure
- Error Protection and Recovery in HW

# Benefits

- AC electrical spec
  - Speeds < 3.5 Gbaud are based on 3.125GBaud XAUI
  - Speeds > 3.5 Gbaud are based on OIF
- Based on industry standards SERDES technology
- Availability of IP
- FPGA support
- Available Expertise

# Benefits – Extended Control Symbol and New Idle



- Provides better CRC protection for DFE based receivers
- Provides auto detection of
  - Lane polarity
  - Differential pair polarity
  - Port width/lane number
  - Data rate capabilities
- Provides mechanism for RX to adjust TX emphasis settings

# Data Plane Feature Overview

- New Data Streaming Packet Format
- Addition of Virtual Channels (VCs) to Serial Physical Layer
- New Endpoint Flow Control Arbitration Spec
- New Traffic Management Spec
- Virtual Output Queue (VoQ) Spec

# Benefits - Data Streaming Support



- Type 9 packet format for streaming data
- Supports up to 64K PDU sizes using selectable MTU size and SAR
- Supports thousands of data streams between endpoints, as well as, concurrent PDUs
- Supports multicast
- Supports lossy transactions
- Introduces COS support with hundreds of traffic classes
- Can be used for encapsulation of any arbitrary protocol

# Benefits – Virtual Channels

- Allows physical channel to be subdivided into independently managed subchannels
  - No ordering guaranteed between VCs
  - Individual link layer flow control and buffers for 9 VCs
- Introduces Continuous Traffic to existing Reliable Traffic
  - Reliable traffic uses VC0, priority based
- Allows reserving of bandwidth and Quality of Service (QoS) on subchannel granularity
  - Scheduling is Implementation defined
- Increases overall utilization of the switch fabric

# Benefits – Flow Control Arbitration



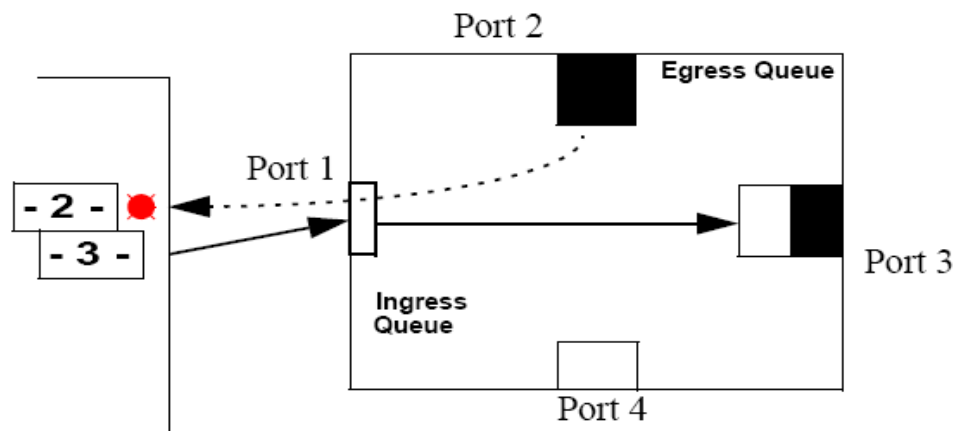
- Extends the existing Type 7 congestion management packet functionality defined for flow level control
- Allows endpoints to manage and arbitrate for resource Segmentation and Reassembly (SAR) contexts at a PDU level
- Prevents traffic from being admitted to the fabric if there are no receiving end resources
- Endpoint wishing to transmit data sends Request message for single or multiple PDUs
- Receiving device allocates (Xon) or de-allocates (Xoff)
- Allows pipeline of request and TX Release message to de-allocate resources

# Benefits – Traffic Management

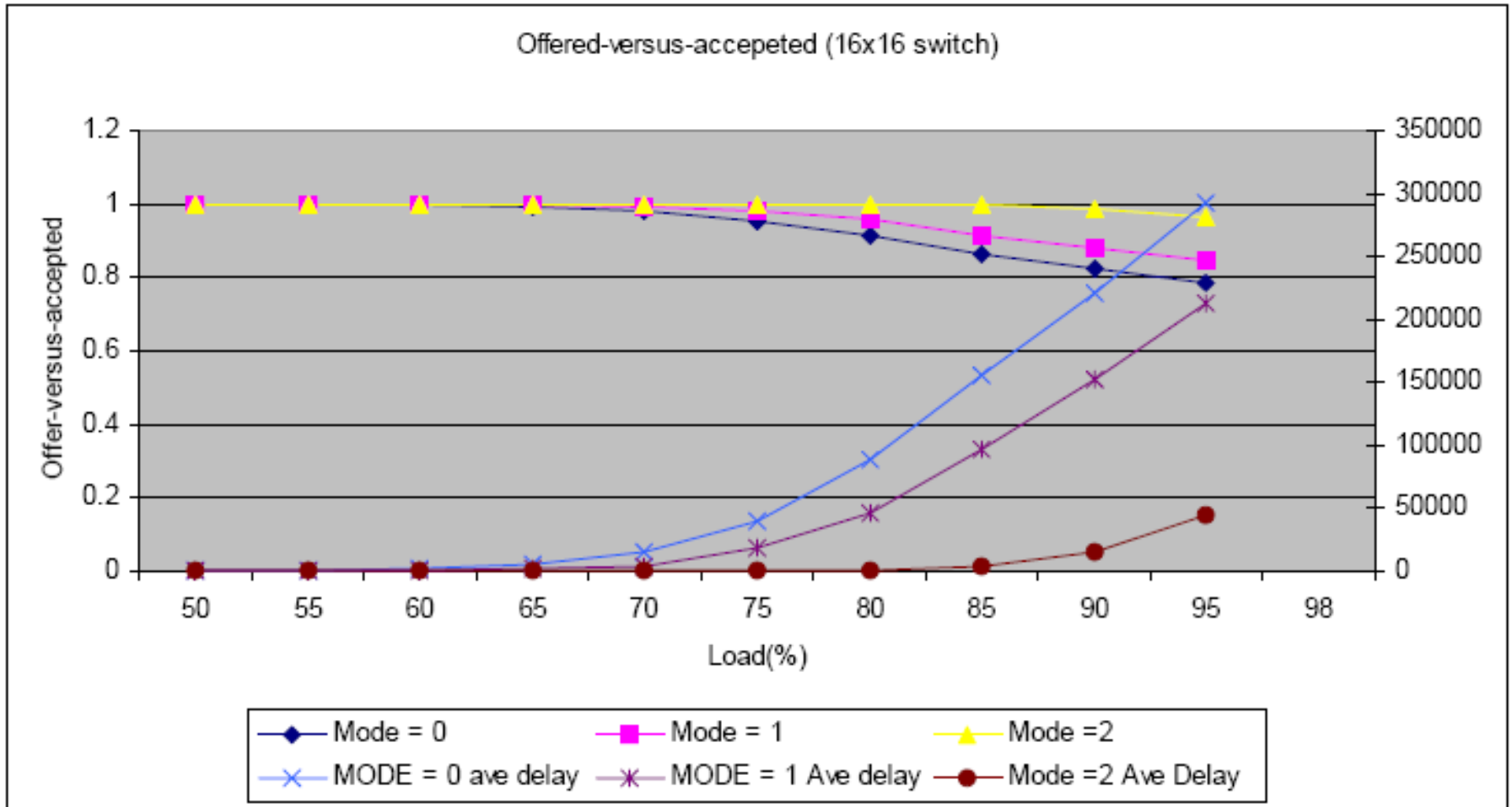
- Allows endpoints to coordinate traffic flows between class and stream based queues
- Uses the extended header type 9 packet format
- Receiving device sends messages to the transmitting device to throttle traffic
- Supports On/Off, Rate based, and Credit based schemes

# Benefits – Virtual Output Queuing

- Method that provides physical layer status messages to communicate congestion status of downstream device's ports.
- Greatly reduces head-of-line (HOL) blocking, increasing fabric performance
- Utilizes the new extended control symbol



# Performance Summary Impact



Courtesy of Erlang Technologies

# Summary



- High Bandwidth, Low Overhead
- Complete Set of Transactions
  - I/O
  - Messaging
  - Globally Shared Memory
  - Streaming Data
- Carrier Grade Data Fabric Performance
  - Deterministic Latency
  - Quality of Service
  - End to End Data Management

Serial RapidIO Gen 2 (2.0 & 2.1)  
Specification Update  
October 2009



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# Contents

- RapidIO 2.0 Specification Review
- Revision 2.1 Enhancements and Impact
- Key 1.3 vs. 2.0 vs. 2.1 Feature Highlights
- Backup Information
  - Full Comparison Table RapidIO 1.3 to Gen2 Specifications

# Revision 2.0 Review

- Public Release in March 2008
- Provides higher performance while maintaining low protocol overhead
- Backwards compatible with 1.3 specification
- Two major areas of concentration
  - New higher performance physical layer
    - 5.0 and 6.25Gbaud rates added with DFE
    - 2x, 8x, and 16x link width options added
    - Data scrambling and new control symbol functionality added
  - Significant Data Plane enhancements
    - Virtual Channels (VCs) added to Serial Physical Layer
    - Virtual Output Queue (VoQ) specification added
    - Data Streaming Packet Format (Type 9 packet)
    - New Endpoint flow control arbitration and traffic management

# Revision 2.1 Enhancements

- Approval in August 2009
- Public release in September 2009
- Goal was to further enhance the specification by enabling additional high speed link implementations and broaden the market applications
- Enhancements include:
  - Mode to facilitate short 5Gbaud links without DFE and with the IDLE1 control symbol
  - Increased robustness of the IDLE2 operation
- These changes will encourage adoption of the higher performance RapidIO specification in a wider range of applications where the conditions demand performance with an aggressive TTM requirement
- The consolidated 2.0/2.1 specification will officially be referred to as Serial RapidIO Gen 2

# Key RapidIO1.3 to Gen2 Feature Comparison

Part	Change Description	1.3 to 2.0	2.0 Spec Section	2.0 to 2.1	2.1 Spec Section
6	Added support for 5 Gbaud and 6.25 Gbaud lane rates	X	Part 6		
6	Added support for 2x, 8x, and 16x ports	X	Part 6 4.6		
6	Support for Virtual Channels 1-8 in physical layer	X	Part 6 2.2		
12	Added Virtual Output Queueing Backpressure specification	X	Part 12		
10	Note that support for Type 9 is optional.	X	Part 10, 1.1		
10	Added 'Extended Header' support to Type 9.	X	Part 10, 4.3		
6	Idle2 Sequence, Long Control Symbols and Data Scrambling Required for 6.25 Gbaud lane rates only.			X	Part 6 3.1

# Backup Information Full Comparison Table RapidIO 1.3 to Gen2 Specifications



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# Revision 1.3 vs. 2.0 vs. 2.1 Detail - 1

Item	Part	Change Description	1.3 to 2.0	2.0 Spec Section	2.0 to 2.1	2.1 Spec Section
1	1	Maintenance read responses with status of ERROR may optionally include data in the response.	X	Part 1, 4.1.10		
2	1	Type 13 packets with status of Error may be either TTYPE 0 or 8, but must not have data.	X	Part 1, 4.2.3		
3	1	Addition of 'Multiport' bit in Processing Element Features CAR.			X	Part 6 6.4.1
4	1	Switch Port Information CAR required if 'Multiport' bit is '1', regardless of the state of bit 3 of the Processing Element Features CAR.			X	Part 6 6.4.1
5	2	Message passing interface annex was specifically labelled as 'informative'	X	Part 2 Annex A		
6	3	Devices must support 'promiscuous mode' for packet reception.	X	Part 3 2.3		
7	3	Recommended that devices always process maintenance read requests, regardless of device ID values.	X	Part 3 2.3		
8	3	Changed requirement for presence of Standard Route Configuration Destination ID Select CSR from bit 23 to bit 22 of the Processing Element Features CAR.	X	Part 3 3.5.4		
9	6	<b>Added support for 2x, 8x, and 16x ports</b>	X	Part 6 4.6		
10	6	<b>Added support for 5 Gbaud and 6.25 Gbaud lane rates</b>	X	Part 6		

# Revision 1.3 vs. 2.0 vs. 2.1 Detail - 2

Item	Part	Change Description	1.3 to 2.0	2.0 Spec Section	2.0 to 2.1	2.1 Spec Section
11	6	Idle2 Sequence, Long Control Symbols and Data Scrambling Required for 5 Gbaud and 6.25 Gbaud lane rates.	X	Part 6 3.1		
12	6	<b>Idle2 Sequence, Long Control Symbols and Data Scrambling Required for 6.25 Gbaud lane rates only.</b>			X	Part 6 3.1
13	6	<b>Support for Virtual Channels 1-8 in physical layer</b>	X	Part 6 2.2		
14	6	Virtual Channel Bandwidth Allocation Register Block	X	Part 6 6.7		
15	6	6 bit ackIDs when IDLE2 Sequence/Long control symbols are used on a link. 5 bit ackIDs when IDLE1 Sequence/Long Control Symbols are used on a link.	X	Part 6 2.2		
16	6	Added VC bit to packet physical layer header	X	Part 6 2.2		
17	6	The ackID field in Packet-Not-Accepted control symbols is undefined	X	Part 6 3.4.3		
18	6	Added 'No Resources' and 'Loss of Descrambler Sync' to the Packet-Not-Accepted cause field.	X	Part 6 3.4.3		
19	6	Added VC Status control symbol type	X	Part 6 3.4.5		
20	6	Added Enter/Exit Loopback control symbol commands to Link Request Control Symbol.	X	Part 6, 3.5.5.1, 3.5.5.2		

# Revision 1.3 vs. 2.0 vs. 2.1 Detail - 3

Item	Part	Change Description	1.3 to 2.0	2.0 Spec Section	2.0 to 2.1	2.1 Spec Section
21	6	Remove Enter/Exit Loopback Control Symbol commands from Link Request Control Symbol.	X	Part 6, 3.5.5		
22	6	Long Control Symbol uses CRC-13.	X	Part 6 3.6.3		
23	6	Optional Baud Rate Discovery feature enabled in the PMA layer.	X	Part 6 4.12.3		
24	6	Support for Adaptive equalization function in the PMA layer.	X	Part 6 4.12.3		
25	6	Definition of Comma	X	Part 6 4.5.6		
26	6	Definition of valid and invalid code-groups			X	Part 6 4.5.6
27	6	Definition of illegal code groups.			X	Part 6 4.5.7.8
28	6	Added use of the Mark ( /M/,  M  ) code group to the IDLE2 sequence	X	Part 6 4.5.7.7		
29	6	All Nx ports must support 1x operation	X	Part 6 4.6		
30	6	All Nx ports must support 'fail down' to redundant 1x operation.	X	Part 6 4.6		

# Revision 1.3 vs. 2.0 vs. 2.1 Detail - 4

Item	Part	Change Description	1.3 to 2.0	2.0 Spec Section	2.0 to 2.1	2.1 Spec Section
31	6	Clarification of IDLE1 sequence definition, always starts with clock compensation sequence, and may be terminated any time after the first 4 characters/columns.	X	Part 6 4.5.9		
32	6	Clarification of IDLE2 sequence			X	Part 6 4.7.4.1.1
33	6	Completely reorganized IDLE2 command fields within the IDLE2 frame.			X	Part 6 4.7.4.1.3
34	6	Requirement for a 250 msec timeout for action on an IDLE2 command.			X	4.7.4.1.4
35	6	1x/2x Mode Detect state machine definition			X	Part 6 4.12.4.4
36	6	All link initialization state machines have changed (ongoing)	X	Part 6 4.12	X	Part 6 4.12
37	6	Increased discovery timer interval to 28 +/- 4 msec			X	Part 6 4.12.4.1.3
38	6	Defined striping rules for ports which are wider than 4x.	X	Part 6 4.10		
39	6	Added concept of reliable traffic (RT) and continuous traffic (CT), linked to VC1-8 operation.	X	Part 6 5.1		
40	6	Rules for scheduling among VCs have been defined.	X	Part 6 5.11		

# Revision 1.3 vs. 2.0 vs. 2.1 Detail - 5

Item	Part	Change Description	1.3 to 2.0	2.0 Spec Section	2.0 to 2.1	2.1 Spec Section
41	6	Specificaton of column padding for 8x & 16x ports	X	Part 6 4.10		
42	6	Detection of a column padding error for 8x & 16x ports (padding characters do not descramble to D0.0 characters)	X	Part 6 5.13.2.1		
43	6	Definition of IDLE2 sequence errors	X	Part 6 5.13.2.2.2		
44	6	Clarification that packets cancelled with a Link-Request control symbol when IDLE2 is active shall have no errors reported if the only errors detected were the presence of /M/ special characters in the packet, and possibly the detection of a packet of excessive length.			X	Part 6, 5.13.2.4
45	6	Clarification that nothing may be transmitted between the data scrambling SYNC sequence and the link-request control symbol.			X	Part 6, 4.8.2
46	6	Reception of a Packet-Retry control symbol when operating in Multi-VC mode.	X	Part 6 5.13.2.3.1		
47	6	Additional error scenarios: Control symbol's start delimiter does not occur in lane number X, where X modulo 4 = 0, and detection of a long control symbol with unequal start and end delimiters	X	Part 6 5.13.2.3.2		

# Revision 1.3 vs. 2.0 vs. 2.1 Detail - 6



Item	Part	Change Description	1.3 to 2.0	2.0 Spec Section	2.0 to 2.1	2.1 Spec Section
48	6	Input error-stopped recovery process extended to cover operation in multi-VC mode, and with reliable/continuous traffic flows	X	Part 6 5.13.2.6		
49	6	Addition of 'Multiport' bit in Processing Element Features CAR.			X	Part 6 6.4.1
50	6	Switch Port Information CAR required if 'Multiport' bit is '1', regardless of the state of bit 3 of the Processing Element Features CAR.			X	Part 6 6.4.1
51	6	Retransmit suppression on error' function removed - Processing element features CAR bit 25 is now implementation specific	X	Part 6 6.4.1		
52	6	Increased field widths in Port n Local ackID CSR to accommodate 6 bit ackIDs	X	Part 6 6.7		
53	6	Port n Error and Status added: Bit 0: IDLE2 support Bit 1: IDLE2 enable Bit 2: Current Idle sequence active Bit 28: Port Unavailable indication	X	Part 6 6.6.8		
54	6	Port n Error and Status added: Bit 4: TX/RX Flow control active			X	Part 6 6.6.8
55	6	Port n Control CSR 16-17: Extended Port-Width override 18-19: Extended Port-Width support 20-27: Changed to implementation defined from 'retransmission suppression mask'	X	Part 6 6.6.9		

# Revision 1.3 vs. 2.0 vs. 2.1 Detail - 7



Item	Part	Change Description	1.3 to 2.0	2.0 Spec Section	2.0 to 2.1	2.1 Spec Section
56	6	Added Port n Control 2 CSR	X	Part 6 6.6.10		
57	6	Added 'Data Scrambling Disable' and 'Inactive Lanes Enable' to Port n Control 2 CSR.			X	Part 6 6.6.10
58	6	Clarification that 'Data Scrambling Disable' does not affect scrambling of D0.0 characters within the IDLE2 random data field			X	Part 6 4.8.1
59	6	Added support for 'Inactive Lanes Enable'			X	Part 6 4.12
60	6	Added LP-Serial Lane Extended Features Block			X	Part 6 6.7
61	6	Added VC Extended Features Block	X	Part 6 6.7		
62	6	Removed packing of VC Extended Features Block registers			X	Part 6 6.8.1
63	6	Signal names changed to allow for up to 16 lanes.	X	Part 6 7		
64	6	Electrical specification clarified for 1.25, 2.5 and 3.125 Gbaud lanes	X	Part 6 Chapters 8, 9		
65	6	Specification of 5.0 and 6.25 Gbaud lanes, short and long reach transmitter.	X	Part 6 Chapter 10		
66	6	Made the input/output common mode voltage identical for short, medium and long reach transmitters/receivers.			X	Part 6, Table 10-2 and 10-6

# Revision 1.3 vs. 2.0 vs. 2.1 Detail - 8



Item	Part	Change Description	1.3 to 2.0	2.0 Spec Section	2.0 to 2.1	2.1 Spec Section
67	6	Added requirement that skew between signals of a differential pair at the transmitter pins must not exceed 15 ps.			X	Part 6 10.4.2.1, 10.4.2.1.5
68	6	BERR rate lowered to 10 <sup>-15</sup> for 5 & 6.25 Gbaud links	X	Part 6, Chapter 8		
69	6	Clarification of how link reinitialization affects link error status, link initialized state and port initialized state.			X	Part 6 5.5.3.1
70	7	Add requirement for promiscuous mode (process packets with any source/destination ID) on exit from reset.	X	Part 7 3.2.1.1		
71	8	Detection of a packet with a destination ID that is undefined is allowed for all processing elements (including switches), not just endpoints.	X	Part 8, 2.3.2.2		
72	8	Requirements for data capture on error are added, including capture of packet/control symbol data, and capture of K/D 10B character indications in the implementation specific field of the Port n Attributes Capture CSR			X	Part 8 1.2.1, 2.3.2
73	8	Modification of physical error rate control and status operation for VC's.			X	Part 8, 1.2.3, 2.3.2
74	8	Clarified which Error Management registers/fields are read only and which are read/write.			X	Part 8, 2.3.2

# Revision 1.3 vs. 2.0 vs. 2.1 Detail - 9



Item	Part	Change Description	1.3 to 2.0	2.0 Spec Section	2.0 to 2.1	2.1 Spec Section
75	8	Clarification of delineation error (29), received illegal or invalid character (15), and received data character in IDLE1 sequence (16) for Port n Error Detect/Enable CSRs			X	Part 8, 2.3.2.10, 2.3.2.11
76	8	Bit 15 and bit 16 are now optional in the Port n Error Detect/Enable CSRs			X	Part 8, 2.3.2.10, 2.3.2.11
77	8	Extension of Port n Attributes Capture CSR to include specification of long control symbol capture			X	2.3.2.12
78	9	Improved explanation of how Flow Control fits in the RapidIO network.	X	Part 9, 1.2		
79	9	Addition of an optional Flow Arbitration protocol with support for Fixed/Static Resource Allocation, and Dynamic Resource Allocation.	X	Part 9, 2.2		
80	10	<b>Note that support for Type 9 is optional.</b>	X	Part 10, 1.1		
81	10	<b>Added 'Extended Header' support to Type 9.</b>	X	Part 10, 4.3		
82	10	Definition of 'Physical Channel ID', and clarification of 'RapidIO flow'.	X	Part 10, 1.5		
83	10	Destinations are permitted to define their use of Virtual Stream IDs to pre-associate certain kinds of traffic with certain end processes.	X	Part 10, 3.2.2		

# Revision 1.3 vs. 2.0 vs. 2.1 Detail - 10



Item	Part	Change Description	1.3 to 2.0	2.0 Spec Section	2.0 to 2.1	2.1 Spec Section
84	10	Added Data Streaming Traffic Management bit 12 to Source/Destination Operations CARs	X	Part 10, 5.4.1, 5.4.2		
85	10	Added bits 0-7 of the Data Streaming Logical Layer Control CSR to control what Flow Arbitration protocol aspects are in use.	X	Part 10, 5.5.1		
86	11	Addition of data streaming error detection to Logical/Transport error detection registers.			X	Part 11 5.4
87	12	<b>Added Virtual Output Queueing Backpressure specification</b>	X	Part 12		

Thank You



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