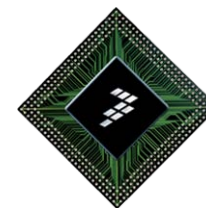




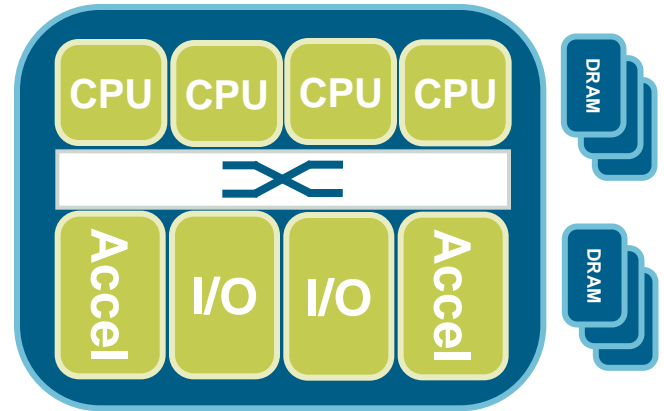
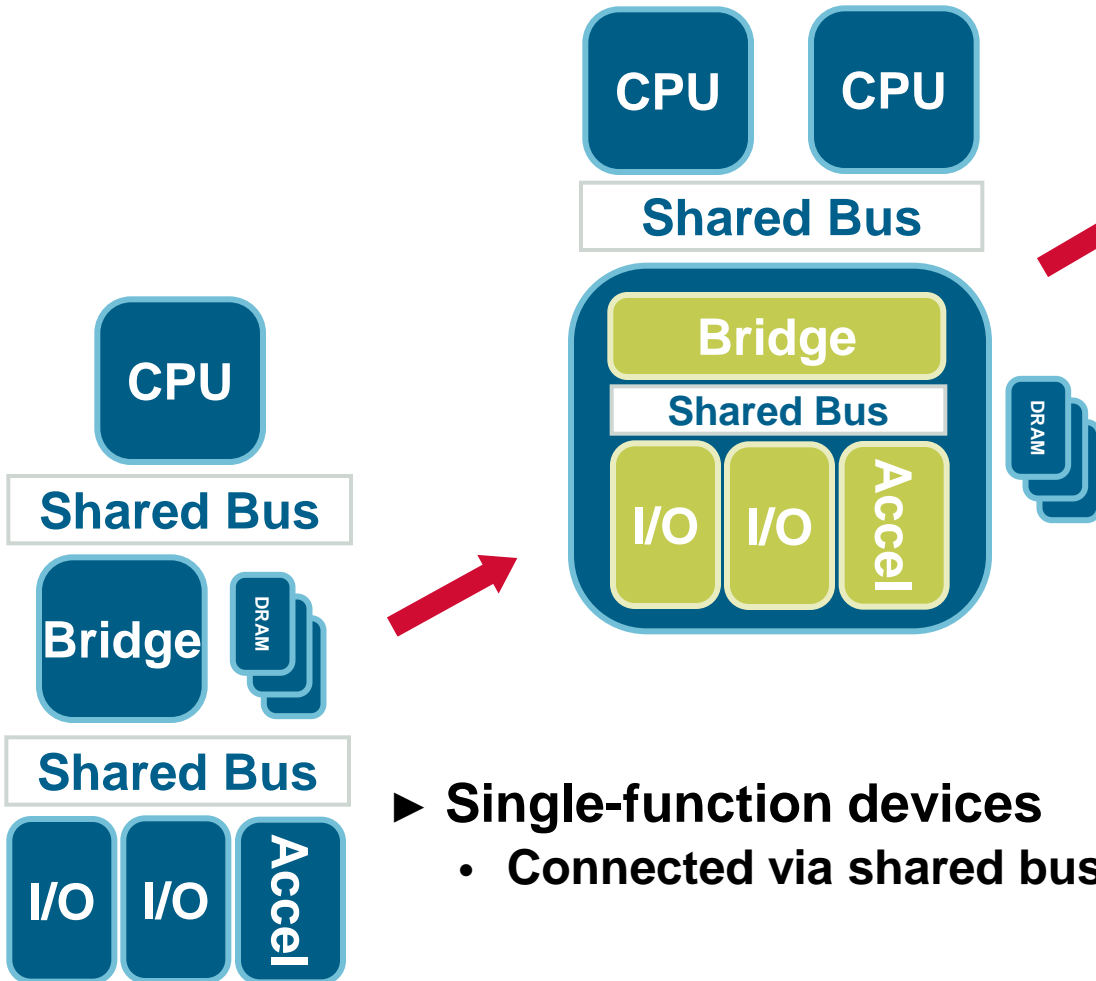
RapidIO Enabling a Multicore World

RapidIO Asia Design Summit, 2009

Jeffrey Ho
AP Technical Marketing
Networking & Multimedia Group



- ▶ **Multi-function device**
 - Limited CPU integration with integrated I/O

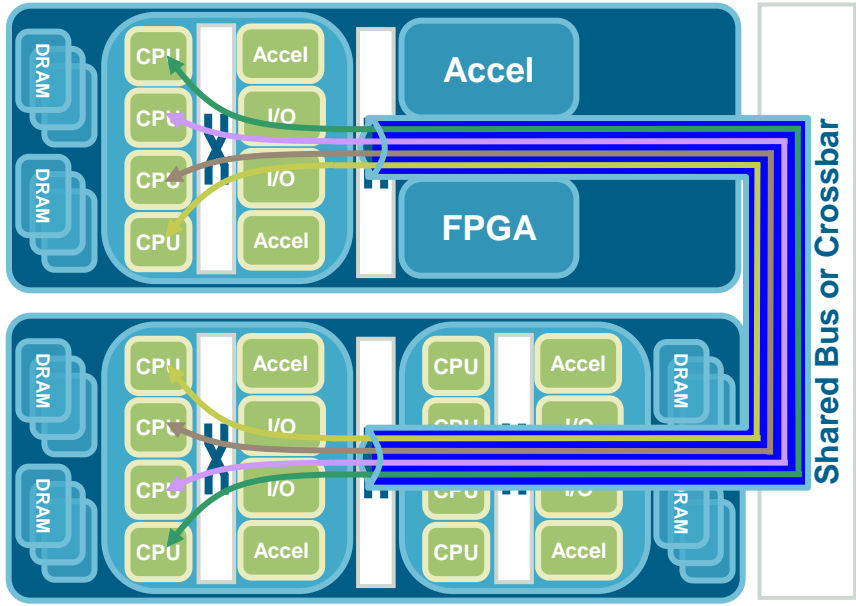
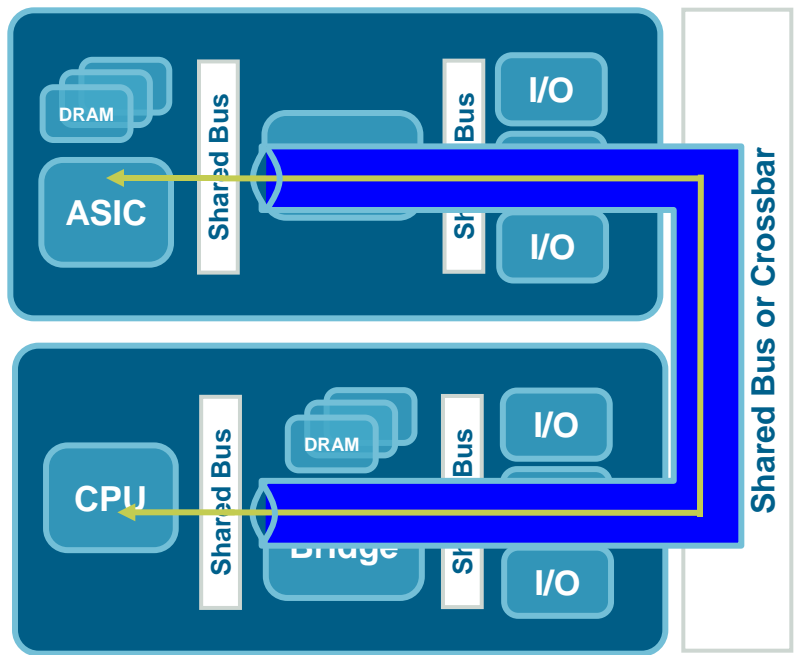


- ▶ **Multicore SoC**
 - Full CPU, accelerator, I/O integration
 - Combined control and data plane functions

- ▶ **Single-function devices**
 - Connected via shared buses

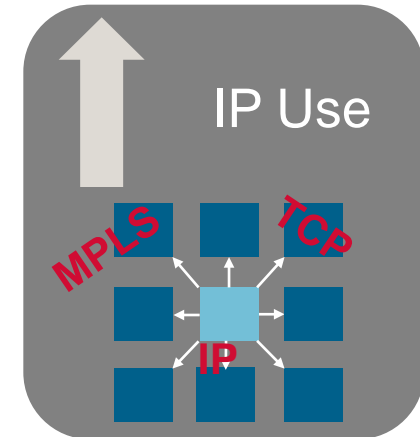
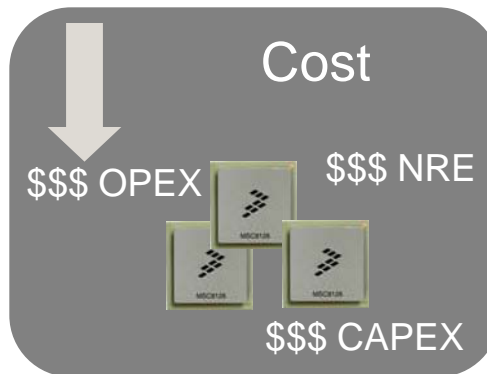
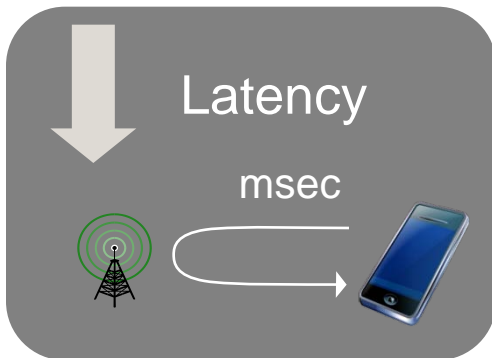
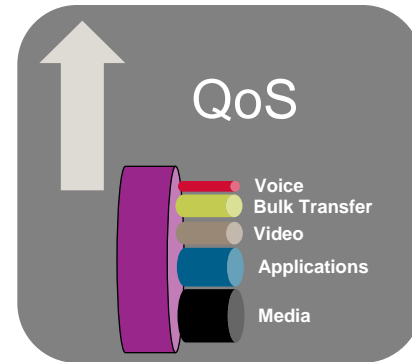
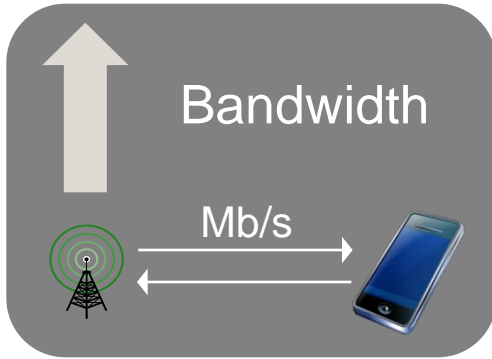
Streams and More Streams

- ▶ **Multicore SoCs**
 - Convergence of control and dataplane
 - Driven by SoC integration trends
 - Many data streams between blocks and silicon devices



- ▶ **Discrete and multi-function silicon**
 - Single data stream between devices

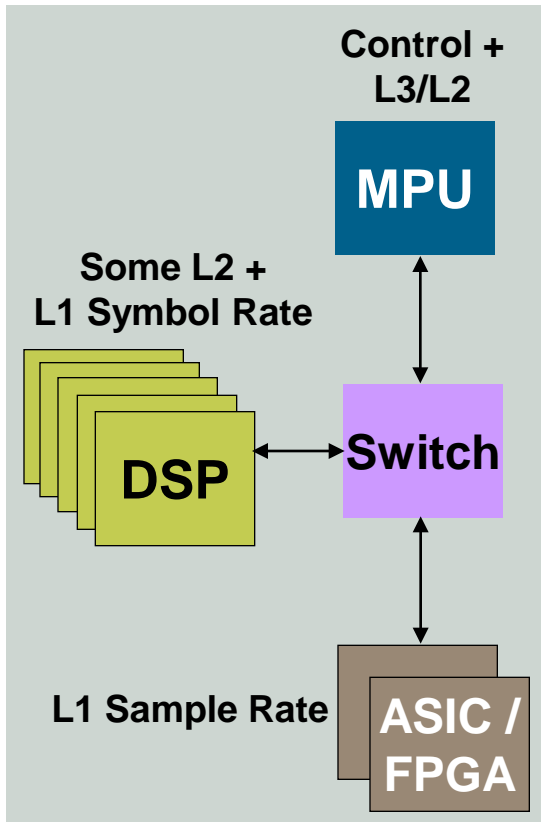
One Application: Wireless Basestation Trends



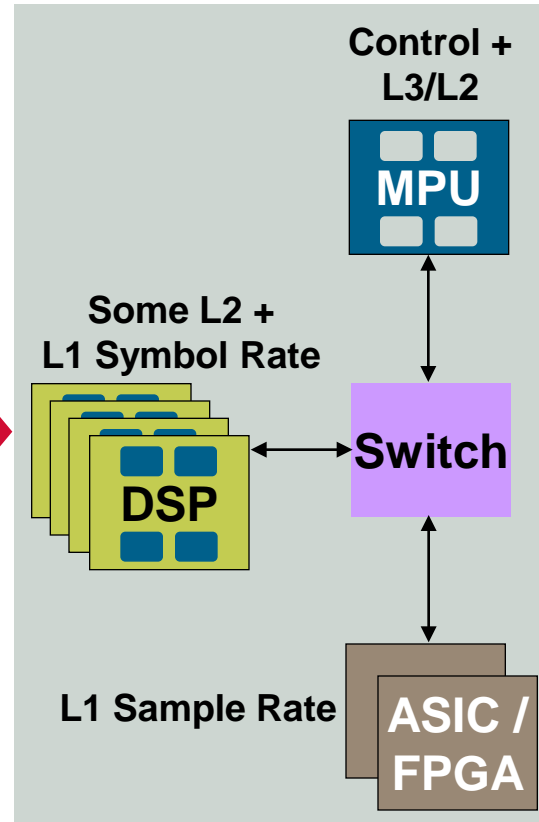
- ▶ Wireless infrastructure a significant driver for innovation in
 - Multicore SoCs
 - System Level Interconnects

Deployment Evolution of Multicore in the BTS

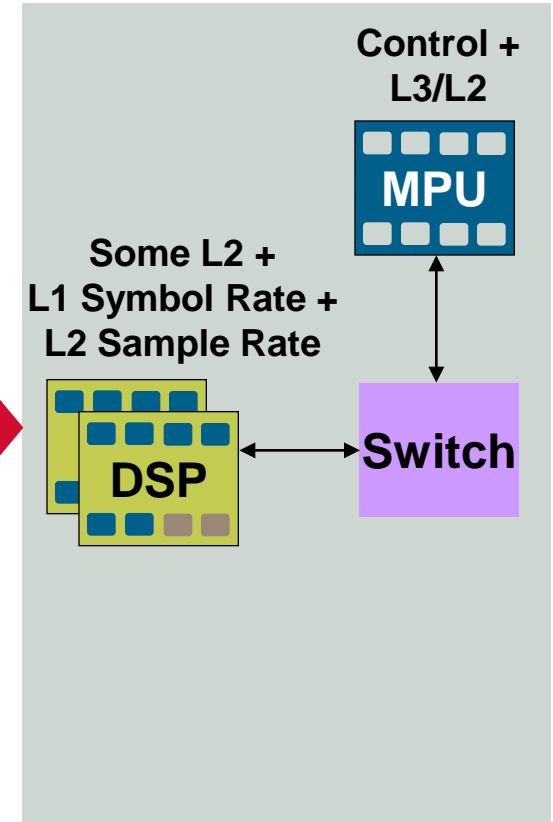
2G



3G-3.5G

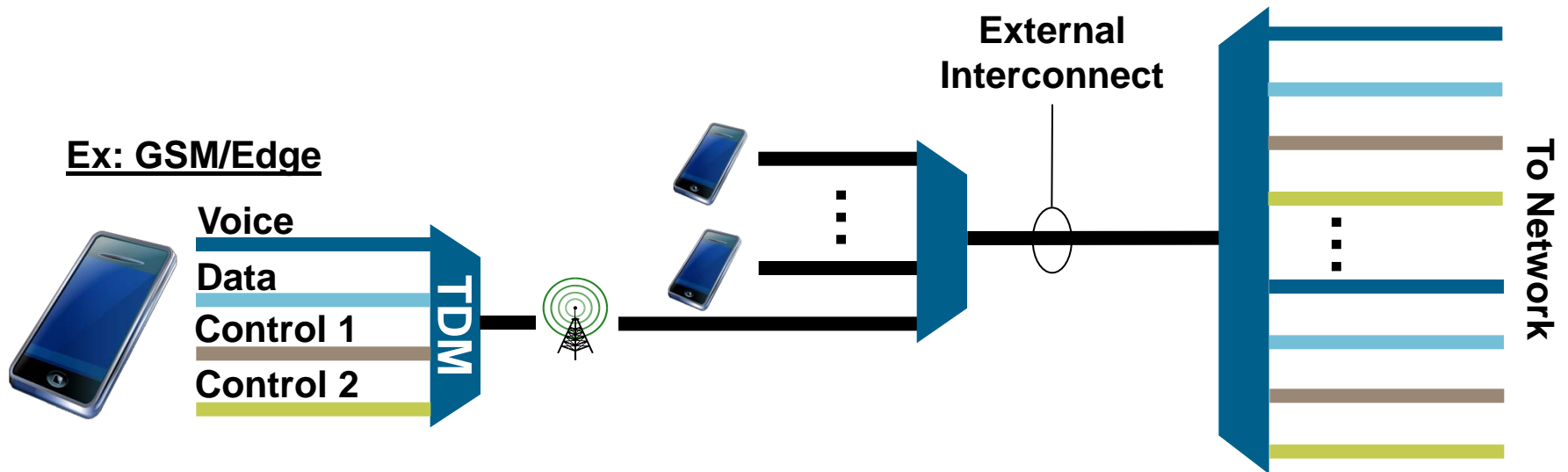


LTE, LTE Future



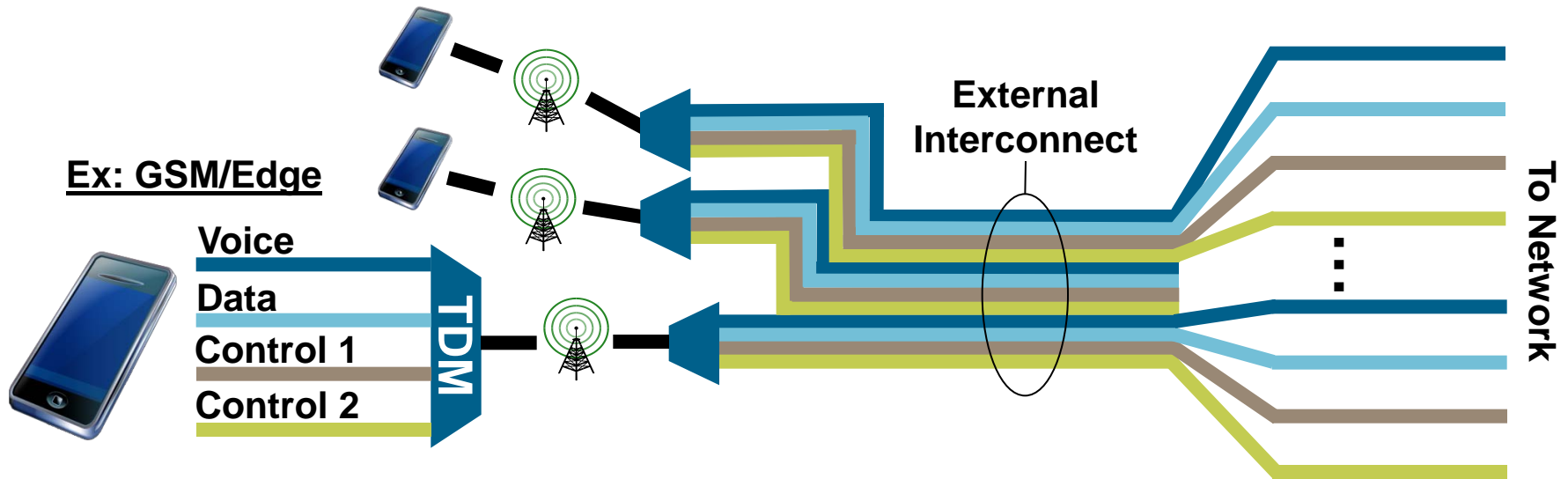
But It's Really About Channelization...

- ▶ Interconnects with native support for streams invokes a virtuous cycle
 - Opportunity to lower mux/demuxing in the system
 - Fewer proprietary headers required for stream differentiation
 - Reduces hardware and software overhead
 - Reduces power



Streaming Support Grows Over Time

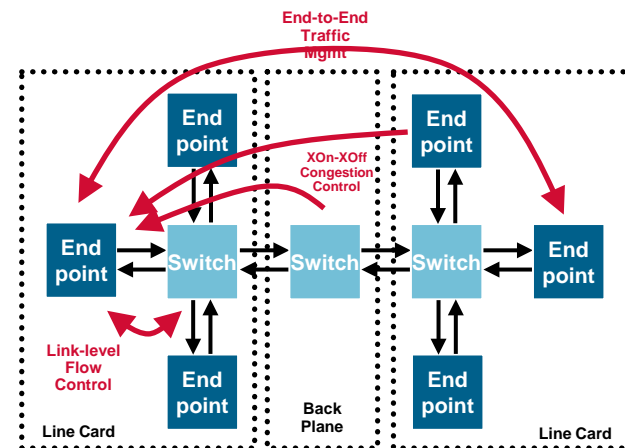
- ▶ Expect unraveling of stream muxing to occur gradually
 - Software won't change overnight even if hardware is supported
 - Multi-stream hardware support must be there first
 - Requires standards to exist ahead of hardware



RapidIO® Is Unique Evolving Logical Layer Standard

► RapidIO leading evolution in logical layer protocols and QoS

- Eight prioritized flows
- Robust Flow Control
 - Link level
 - Congestion to Source
 - End-to-end (Traffic Management)
- Type 11 Messaging Transaction Type
 - 4KB Max User PDU
 - 16 Streams Max per Flow
- Type 9 Data Streaming Transaction Type
 - 64 KB Max User PDU
 - 256 Classes-of-Service (CoS) per flow
 - 65,536 Streams/CoS per flow
 - Standardized Traffic Management
 - Stream setup/teardown
 - End-to-end Flow Control
 - Encapsulation

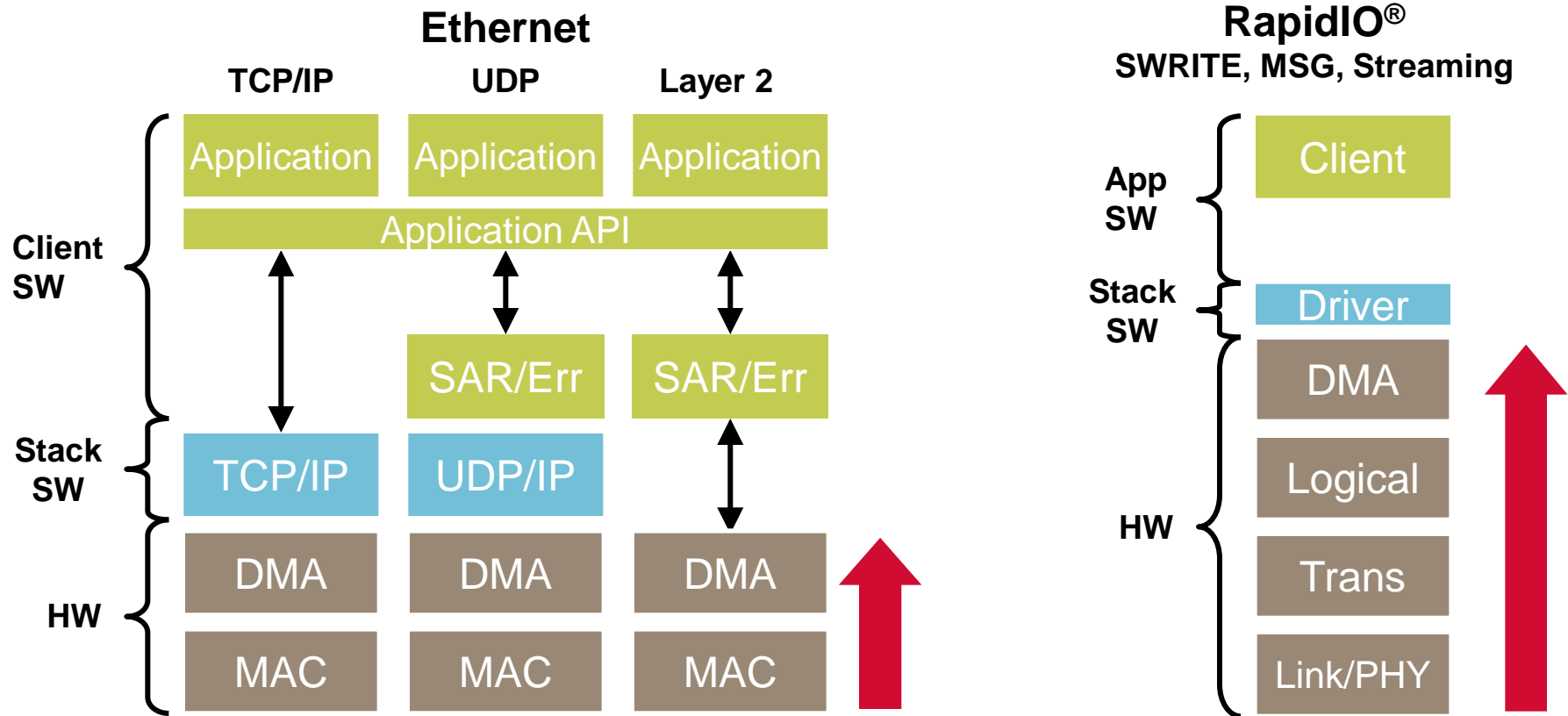


Type 11 Packet



Type 9 Packet






















It's the Logical Layer...



► Applications driving innovation at logical layer of interconnects

- Off-load moving upward in the stack
 - Logical layer implemented in hardware
 - Ethernet example of when this isn't the case
 - Power, performance and QoS are drivers

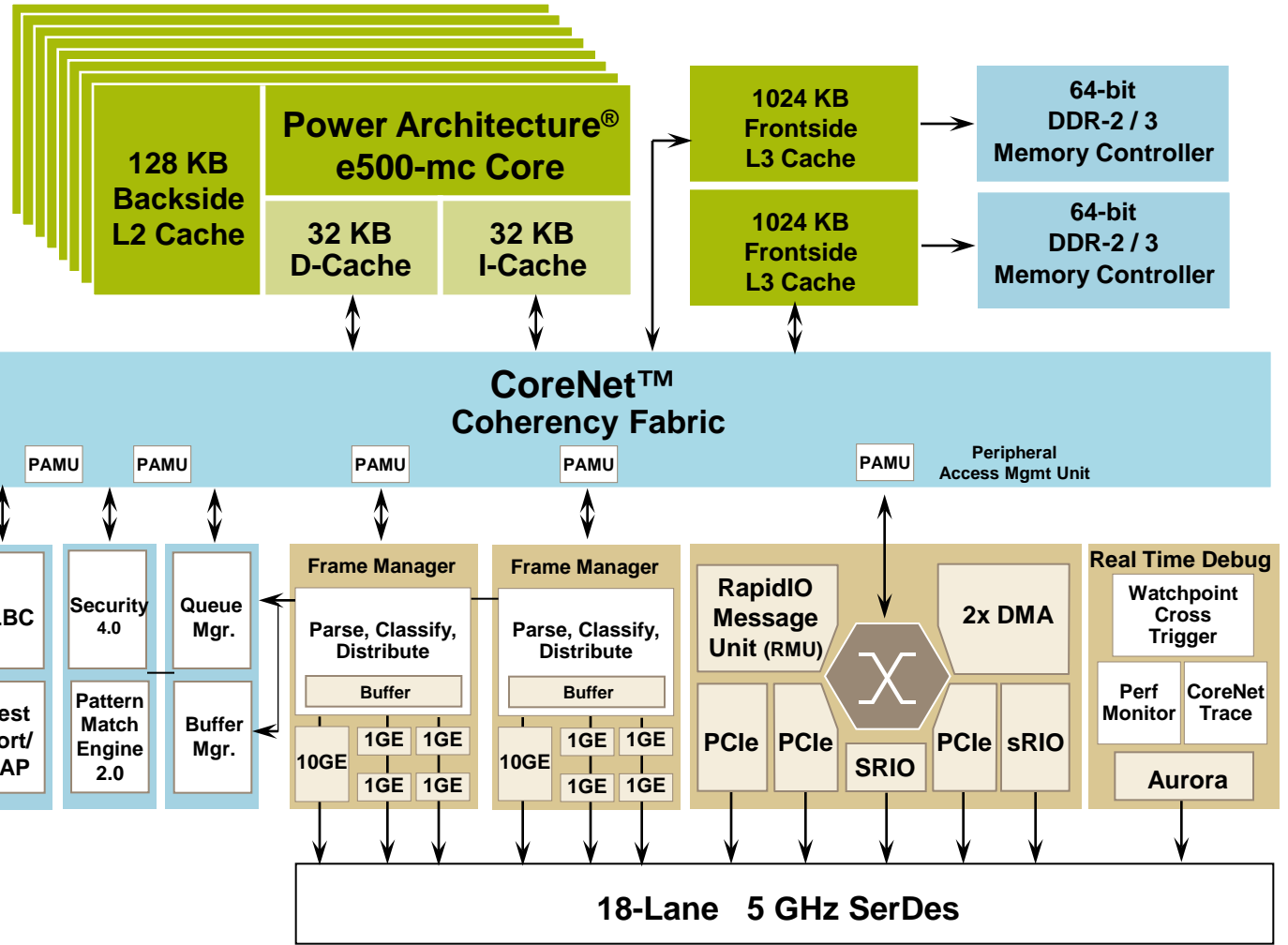
QorIQ™ Platform Levels

PLATFORMS / PRODUCTS	DESCRIPTION	APPLICATION EXAMPLES
<p>QorIQ P5 PRODUCTS: To be announced</p> 	<p>Highest-performing embedded processors</p>	   <p>Service Provider Routers Network Admission Control Storage Networks</p>
<p>QorIQ P4 PRODUCTS: P4080</p> 	<p>Tap the full potential of multicore with this “many-core” platform</p>	    <p>Metro Carrier Edge Router IMS Controller Radio Network Control Serving Node Router (GSN)</p>
<p>QorIQ P3 PRODUCTS: To be announced</p> 	<p>Your first step into true multicore performance</p>	   <p>Converged Media Gateway SSL, IPSec, Firewall Access Gateway</p>
<p>QorIQ P2 PRODUCTS: P2020 P2010</p> 	<p>Unprecedented performance per watt in this highly integrated platform</p>	    <p>Unified Threat Management VoIP Carrier-Class Media Gateway Wireless Media Gateway Basestation</p>
<p>QorIQ P1 PRODUCTS: P1020 P1011</p>	<p>A highly integrated, cost-effective, low power platform</p>	   <p>Integrated Services Router Network Attached Storage Home Media Hub</p>



QorIQ™ P4 Series P4080 Block Diagram

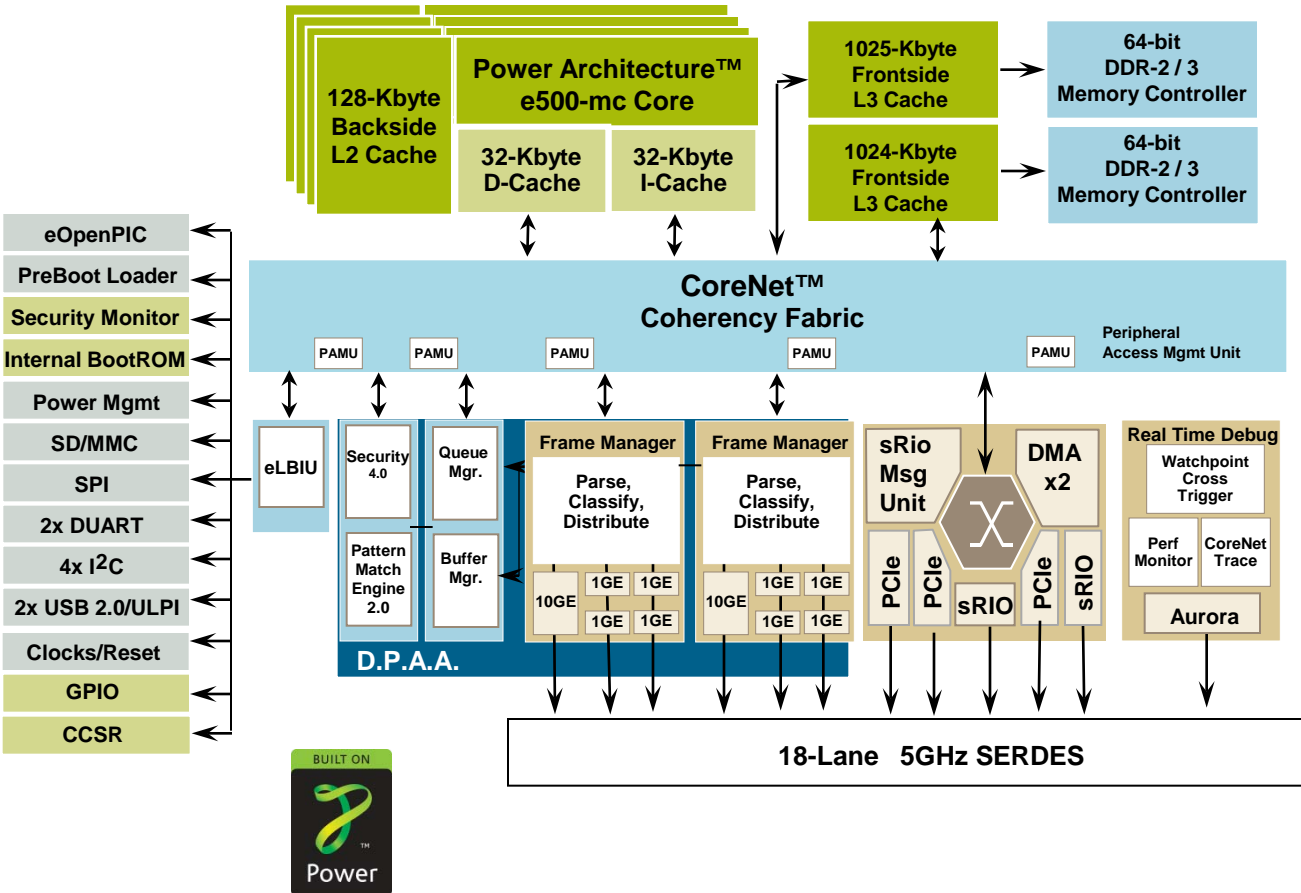
QorIQ™ P4080 MULTICORE PROCESSOR



- eOpenPIC
- PreBoot Loader
- Security Monitor
- Internal BootROM
- Power Mgmt
- SD/MMC
- SPI
- 2x DUART
- 4x I²C
- 2x USB 2.0/ULPI
- Clocks/Reset
- GPIO
- CCSR

QorIQ™ P4 Series P4040 Block Diagram

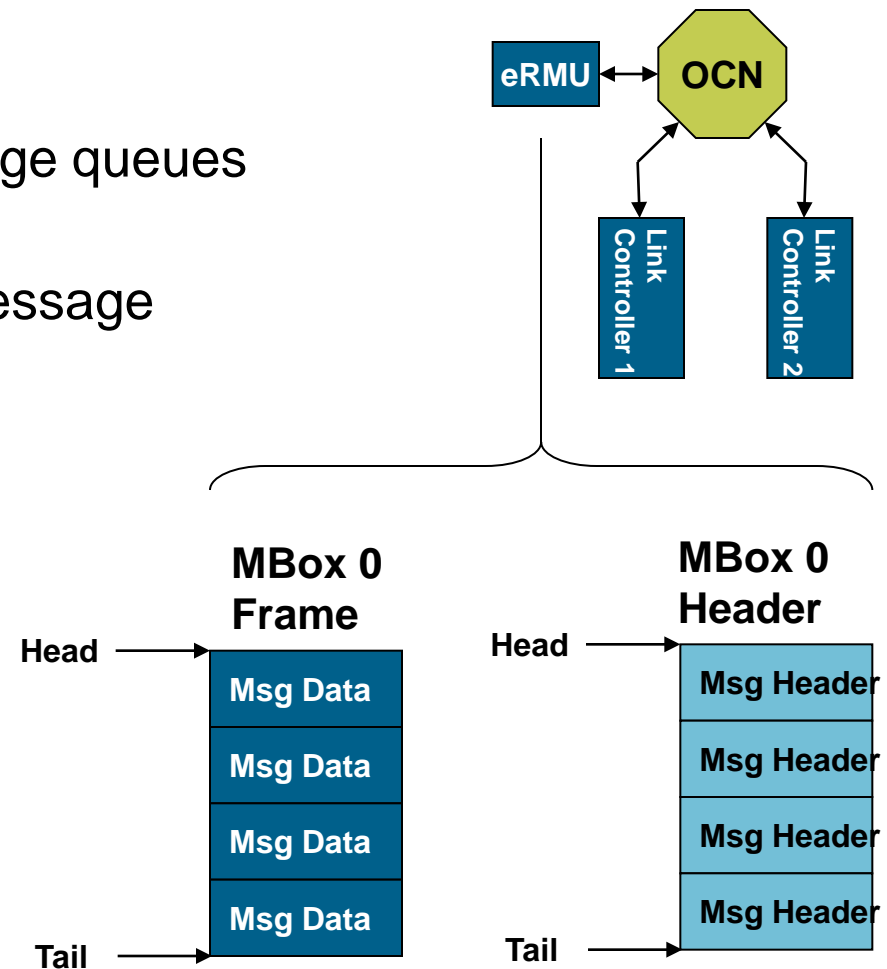
QorIQ™ P4040 MULTICORE PROCESSOR



- ▶ **Quad e500mc Power Architecture®**
 - 4 cores (up to 1.5GHz)
 - Each with 128KB backside L2 cache
 - 2 MB Shared L3 Cache w/ECC
- ▶ **Memory Controller**
 - DDR2/3 SDRAM up to 1.6 GHz
 - 32/64 bit data bus w/ECC
- ▶ **High Speed Interconnect**
 - 3 PCIe 2.0 Controllers
 - 2 serial RapidIO Controllers
- ▶ **CoreNet™ Switch Fabric**
- ▶ **Ethernet**
 - 8 x 10/100/1000 Ethernet Controllers
 - 2 x 10GE Controllers
 - Classification/Policing, H/W Queuing, policing, and Buffer Management, Checksum Offload, QoS, Lossless Flow Control, IEEE 1588, SGMII/XAUI
- ▶ **Datapath Acceleration**
- ▶ **Device**
 - 45nm SOI Process
 - 1295-pin package, pin compat with P4080
 - 30-35% lower power than P4080

Enhanced RapidIO Interface for P4080, P4040

- ▶ Dual Rev 1.2 link controllers
- ▶ Single “eRMU” messaging unit
 - Dual inbound and outbound message queues
- ▶ New mailbox header queue
 - Carries header information from message
 - Source ID
 - prio (Flow)
 - mbox
 - xmbox
 - Letter
 - Length (multiples of 8 bytes)



Dual-core P2020 Block Diagram

- **Dual e500 cores built on Power Architecture® technology**

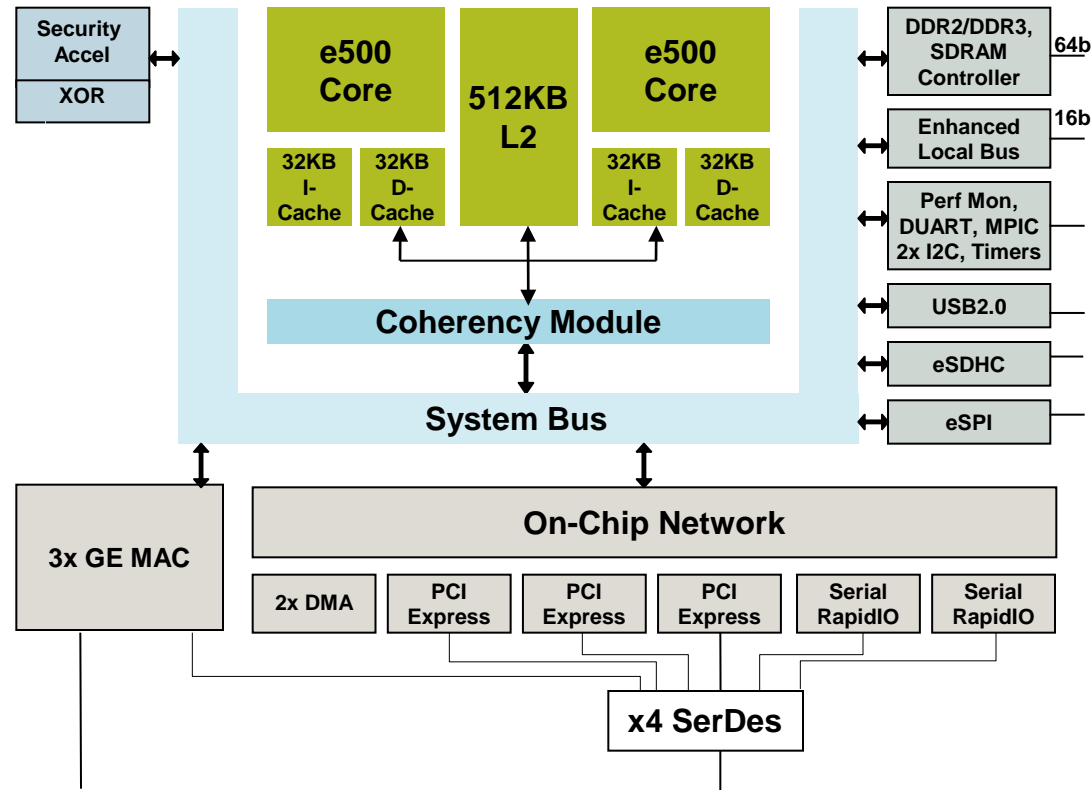
- 800 - 1200 MHz
- 512 KB Frontside L2 cache w/ECC, HW cache coherent
- 36-bit physical addressing, DP-FPU

- **System Unit**

- 64-/32-bit DDR2/DDR3 with ECC
- Integrated SEC 3.1 Security Engine
- Open-PIC Interrupt Controller, Perf Mon, 2x I²C, Timers, 16 GPIO's, DUART
- 16-bit Enhanced Local Bus supports booting from NAND Flash
- One USB 2.0 Host Controller with ULPI interface
- SPI controller supporting booting from SPI serial Flash
- SD/MMC card controller supporting booting from Flash cards
- Three 10/100/1000 Ethernet Controllers (eTSEC) w/ Jumbo Frame support, SGMII interface
 - Enhanced features: Parser/Filer, QOS, IP-Checksum Offload, Lossless Flow Control
 - IEEE® 1588v2 support
- Two Serial RapidIO® controllers with integrated message unit operating up to 3.125 GHz
- Three PCI Express® 1.0a Controllers operating at 2.5 GHz

- **Process and Package**

- 45 nm SOI, 1.05V +/- 50mV, 0C to 125C Tj
 - with -40C to 125C Tj option
- 689-pin TEPBGAI, 31x31mm



Single-Core P2010 Block Diagram

- **Single e500 core, built on Power Architecture® technology**

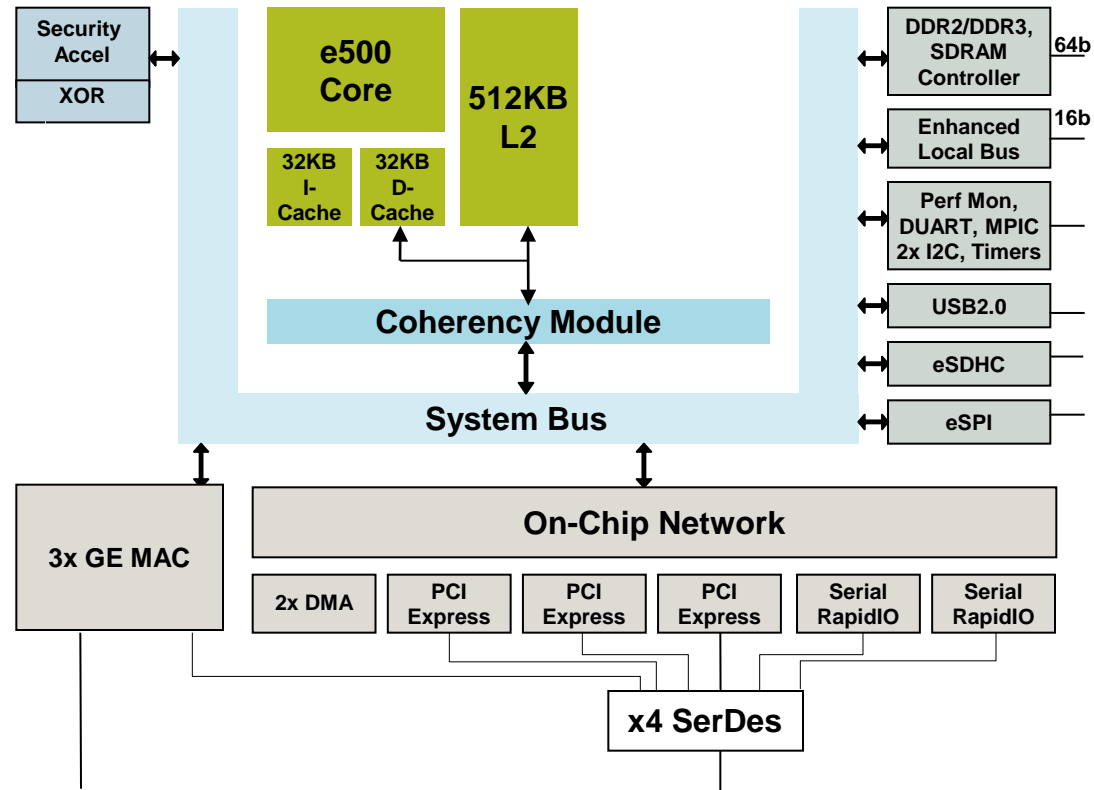
- 800 – 1200 MHz
- 512 KB Frontside L2 cache w/ECC, HW cache coherent
- 36-bit physical addressing, DP-FPU

- **System Unit**

- 64-/32-bit DDR2/DDR3 with ECC
- Integrated SEC 3.1 Security Engine
- Open-PIC Interrupt Controller, Perf Mon, 2x I²C, Timers, 16 GPIO's, DUART
- 16-bit Enhanced Local Bus supports booting from NAND Flash
- One USB 2.0 Host Controller with ULPI interface
- SPI controller supporting booting from SPI serial Flash
- SD/MMC card controller supporting booting from Flash cards
- Three 10/100/1000 Ethernet Controllers (eTSEC) w/ Jumbo Frame support, SGMII interface
 - Enhanced features: Parser/Filer, QOS, IP-Checksum Offload, Lossless Flow Control
 - IEEE® 1588v2 support
- Two Serial RapidIO® controllers with integrated message unit operating up to 3.125 GHz
- Three PCI Express® 1.0a Controllers operating at 2.5 GHz

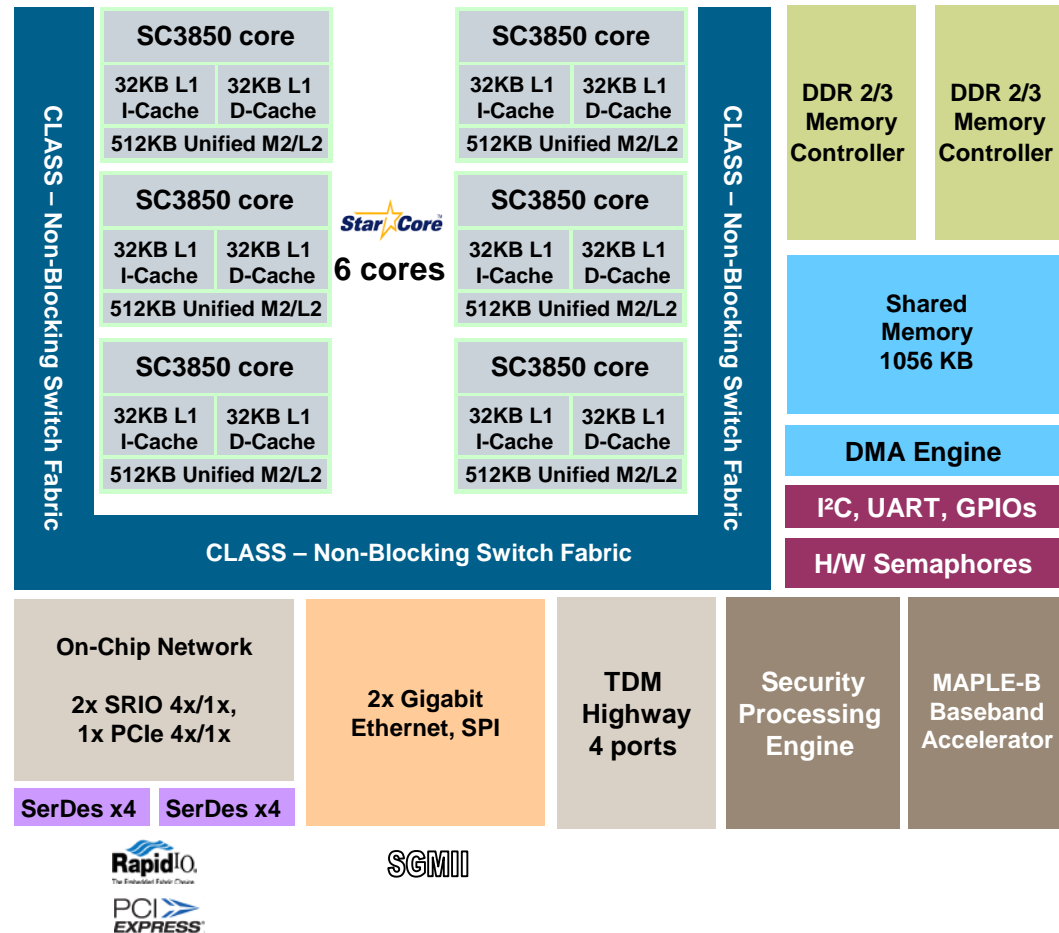
- **Process and Package**

- 45 nm SOI, 1.05V +/- 50mV, 0C to 125C Tj
 - with -40C to 125C Tj option
- 689-pin TEPBGAll, 31x31mm



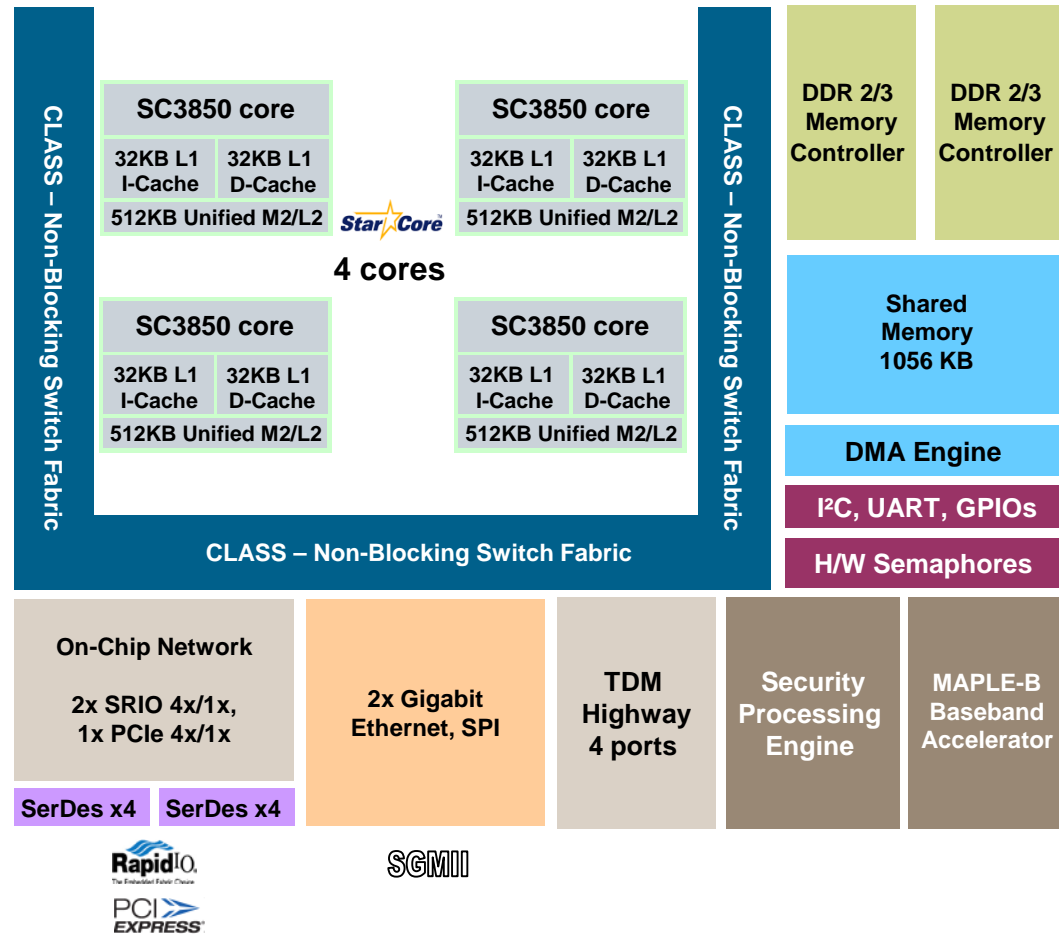
MSC8156/E – Broadband Wireless DSP

- **6x SC3850 Cores Subsystems (6GHz/48GMACS) each with:**
 - SC3850 DSP core at up to 1GHz (8GMACS 16b or 8b)
 - 512 Kbyte unified L2 cache / M2 memory.
 - 32 Kbyte I-cache, 32Kbyte D-cache, WBB, WTB, MMU, PIC
- **Internal/External Memories/Caches**
 - 1056 KByte M3 shared memory (SRAM)
 - Two DDR 2/3 64-bit SDRAM interfaces at up to 800 MHz
- **CLASS – Chip-Level Arbitration & Switching Fabric**
 - Non-Blocking, fully pipelined, low latency
 - Full fabric 12 masters to 8 slaves, up to 512 Gbps throughput
- **MAPLE-B – Baseband Accelerator**
 - Turbo/Viterbi Decoder up to 200/115 Mbps
 - Fourier Transform accelerator up to 350 Msps FFT and 175 Msps DFT
 - Supporting: 3G-LTE, 802.16, 3G, CDMA2K standards
- **Security Engine (Talitos 3.1)**
 - Data and Code Protection (AES, SHA, RC-4, Kasumi, SNOW)
- **High Speed Interconnects**
 - Dual 4x/1x Serial RapidIO at 1.25/2.5/3.125 Gbaud
 - PCI-e 4x/1x
- **Dual RISC QUICCEngine® supporting**
 - Dual SGMII/RGMII Gigabit Ethernet ports
 - Eth. Protocols, Talitos control and sRIO offload
- **TDM Highway**
 - 1024 ch., 400Mbps, divided into 4 ports of 256
- **DMA Engine 16 bi-directional channels**
- **8 hardware semaphores**
- **Other Peripheral Interfaces**
 - SPI, UART, I2C, 32 GPIO, 16 Timers, 96KB boot ROM, JTAG/SAP, 8WDT
- **Technology**
 - 45nm SOI, 1V core, 2.5, 1.8/1.5V I/O
 - FCBPGA (29x29) 1mm pitch, RoHS



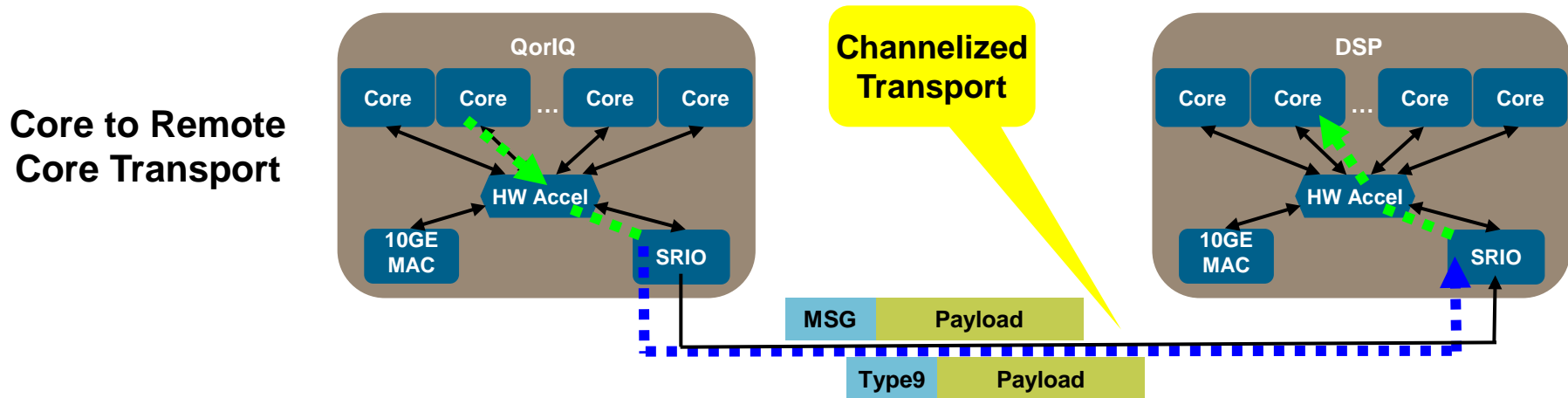
MSC8154/E – Broadband Wireless DSP

- **4x SC3850 Cores Subsystems (4GHz/32GMACS) each with:**
 - SC3850 DSP core at up to 1GHz (8GMACS 16b or 8b)
 - 512 Kbyte unified L2 cache / M2 memory.
 - 32 Kbyte I-cache, 32Kbyte D-cache, WBB, WTB, MMU, PIC
- **Internal/External Memories/Caches**
 - 1056 KByte M3 shared memory (SRAM)
 - Two DDR 2/3 64-bit SDRAM interfaces at up to 800 MHz
- **CLASS – Chip-Level Arbitration & Switching Fabric**
 - Non-Blocking, fully pipelined, low latency
 - Full fabric 12 masters to 8 slaves, up to 512 Gbps throughput
- **MAPLE-B – Baseband Accelerator**
 - Turbo/Viterbi Decoder up to 145/160 Mbps
 - Supporting: 3G-LTE, 802.16, 3G, CDMA2K standards
 - Fourier Transform accelerator up to 200 Msp/s FFT and 175 Msp/s DFT
- **Security Engine (Talitos 3.1)**
 - Data and Code Protection (AES, SHA, RC-4, Kasumi, SNOW)
- **High Speed Interconnects**
 - Dual 4x/1x Serial RapidIO at 1.25/2.5/3.125 Gbaud
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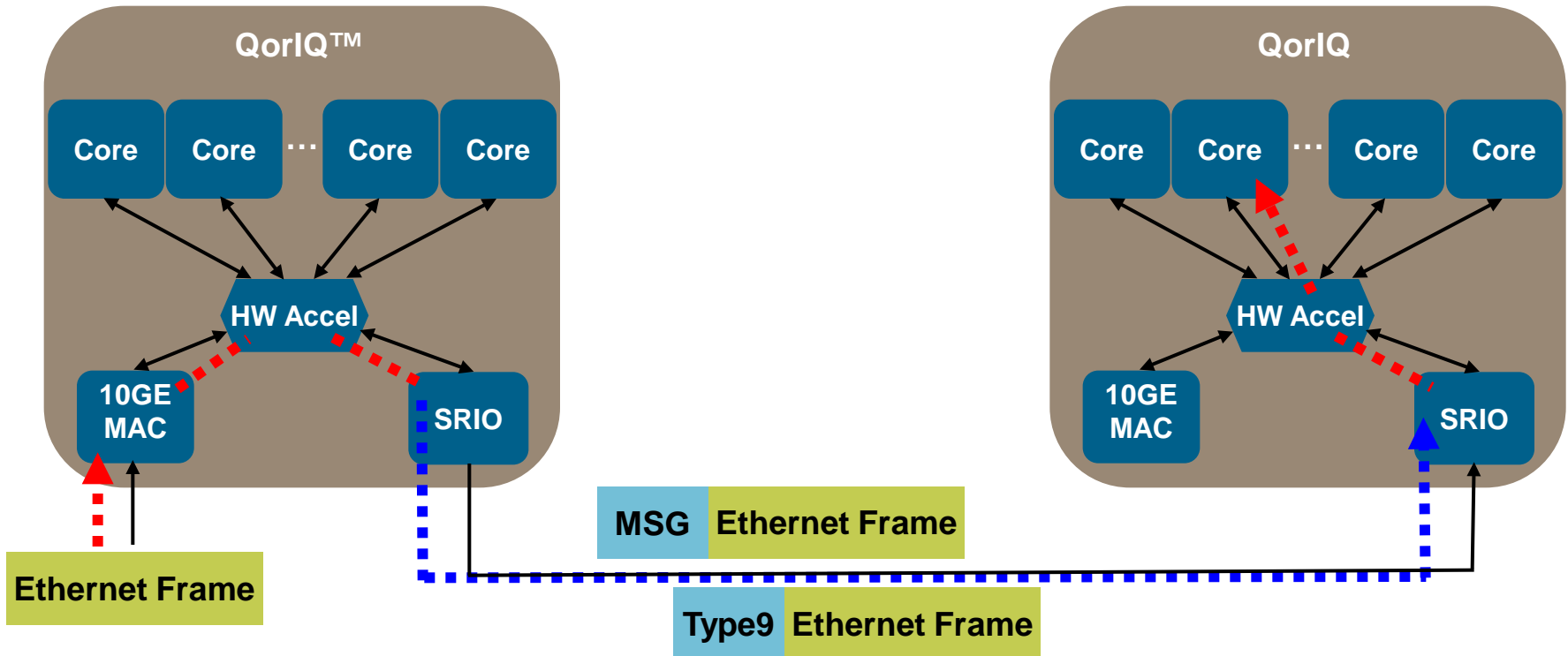


Next Gen RapidIO® for Freescale Multicore Processors

- ▶ Virtualizes RapidIO data transfers for QorIQ™
 - Very low CPU overhead
 - Enables zero overhead direct core-to-core communication
- ▶ Supports all messaging-style transaction types
 - Type 11 Messaging
 - Type 10 Doorbells
 - Type 9 Data Streaming
- ▶ Many queues allow multiple inbound/outbound queues per core
 - Hardware queue management via QorIQ Datapath Architecture (DPAA)
- ▶ Enhanced QoS
 - End-to-end per stream flow control

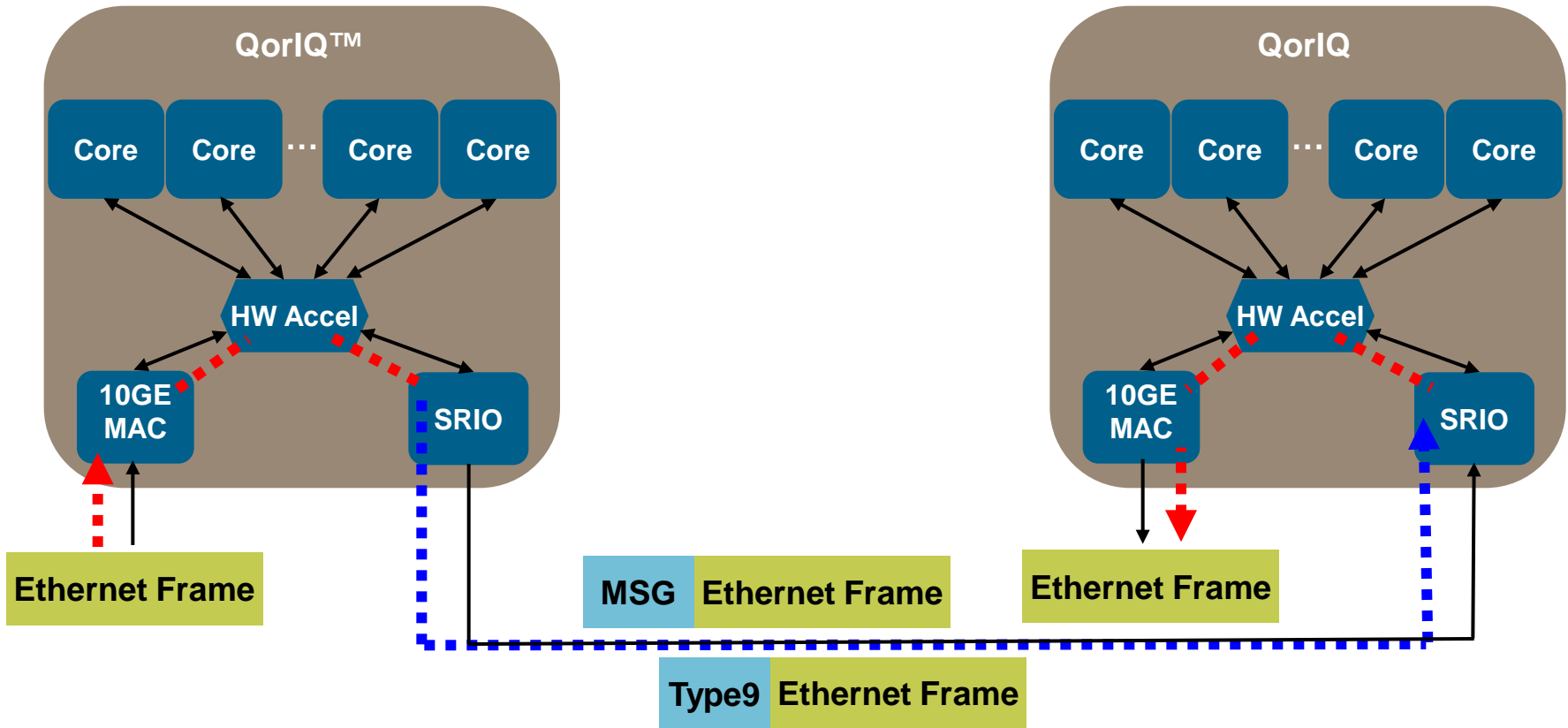


New Use Models: Scalable Multicore System



- ▶ Ethernet to Remote CPU Transport
- ▶ Virtualizes core-as-a-resource across devices
- ▶ Zero-CPU Overhead

New Use Models: Transparent Ethernet Bridging

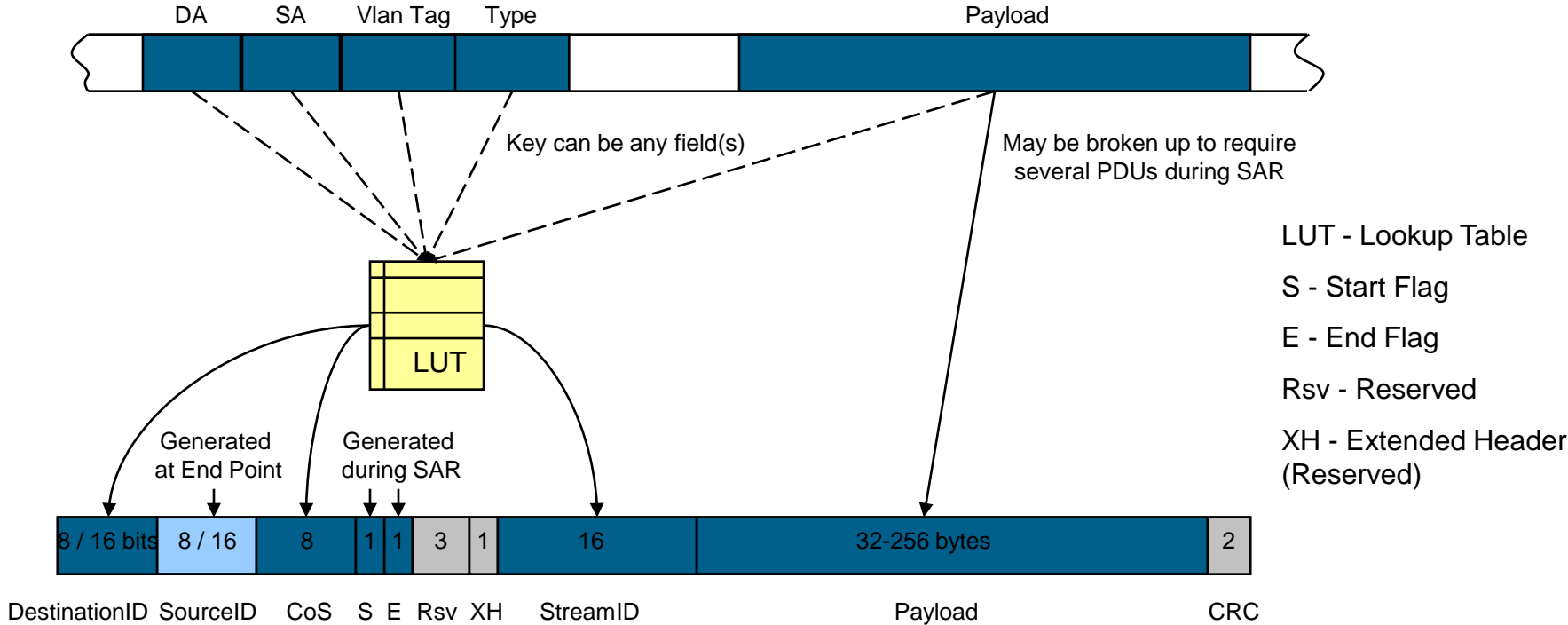


- ▶ Zero-CPU Overhead
- ▶ Ethernet Classification supported

Encapsulating Protocols

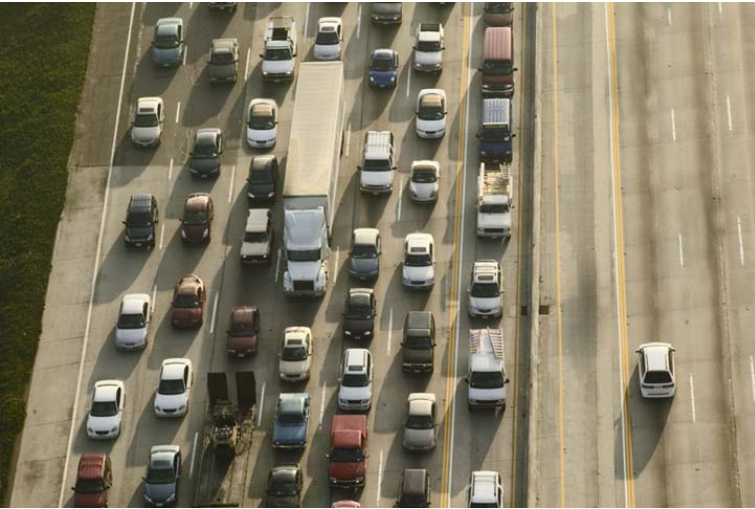
Possible implementation of encapsulating a **Ethernet** frame into a RapidIO Data Streaming PDU

GMII Frame



Rapid IO Data Streaming PDU (start segment)

Conclusion



- ▶ **System requirements and the emergence of multicore devices point to increasing channelization**
- ▶ **RapidIO leads the industry in its support for channelization and multicore support**
- ▶ **Freescale leads the market in RapidIO support across our product lines**
- ▶ **New Freescale RapidIO controller innovations will enable unique low-overhead use models**



Technology that Changes Our World

