

Flexible interconnection with serial RapidIO on TI high performance DSP

Oct., 2009

Texas Instruments

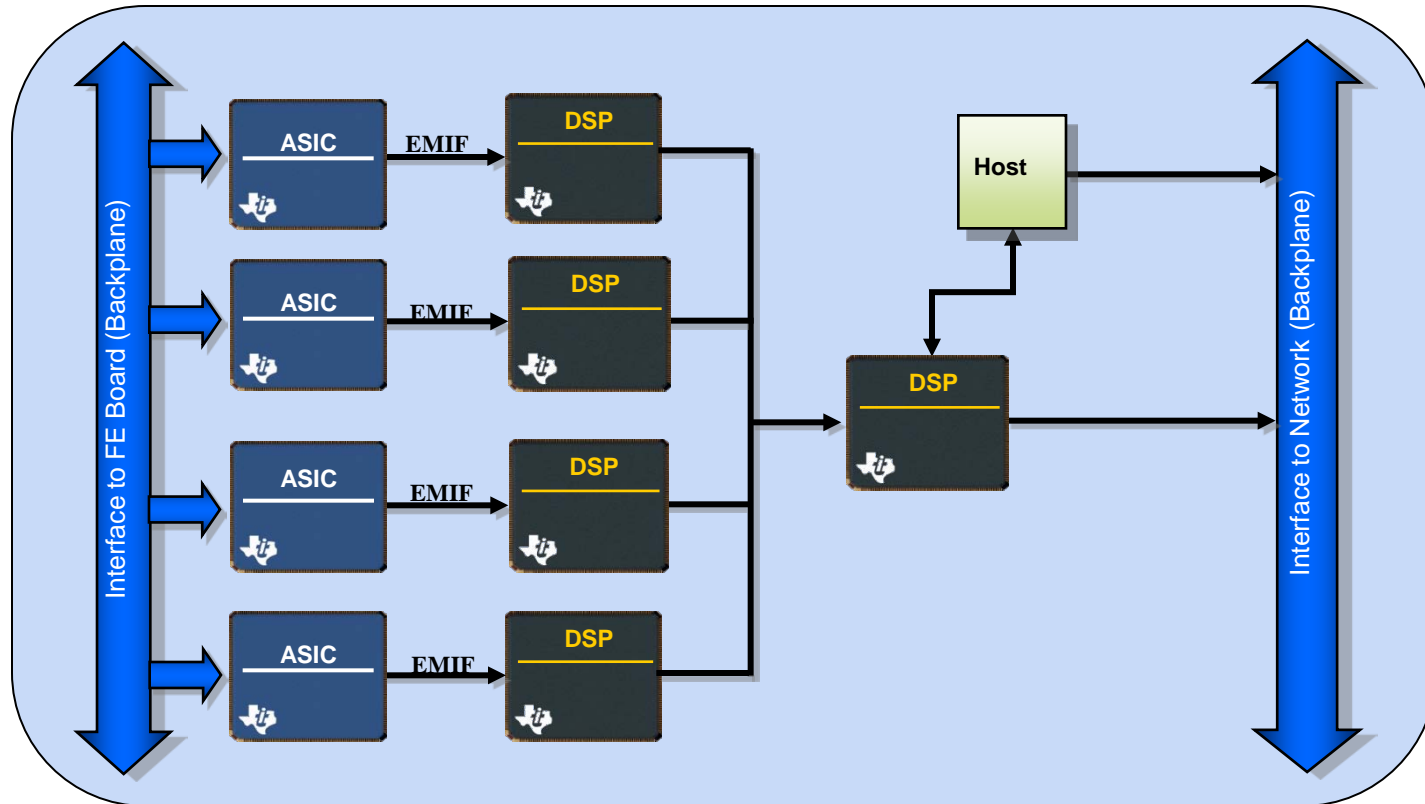
Agenda

- Interface Requirements for High Performance DSP
- Past & present DSP interconnects
- RapidIO Advantages
- DSP Interconnection with SRIO
- Available SRIO DSP Processors in TI
- Summary

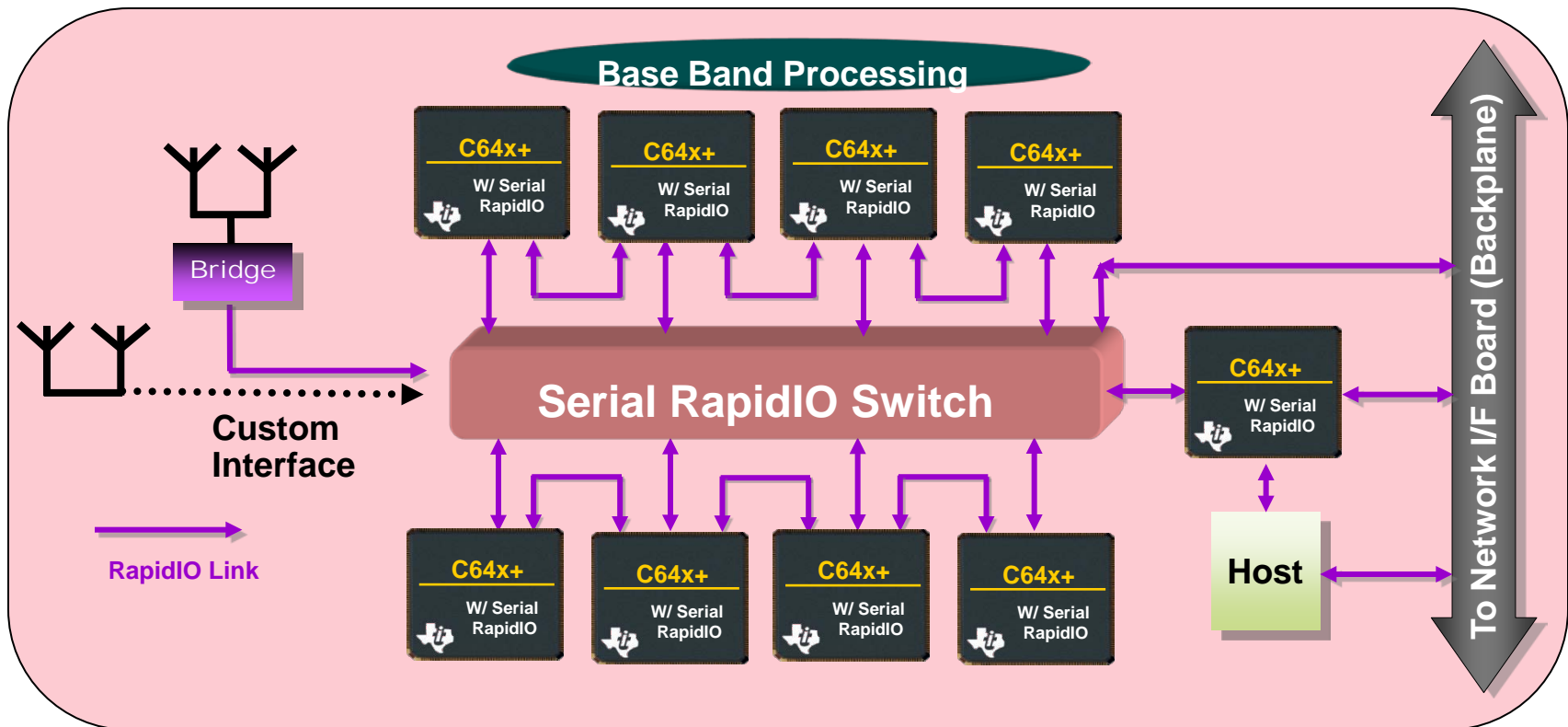
Interface on TI High performance DSP

- Why we need high data throughput interface on high performance DSP?
- What kind of interfaces are fit for high performance DSP?
- High data throughput interfaces on TI high performance DSP
 - Ethernet
 - Serial RapidIO

Past interconnection based on TI DSP for Baseband application



Current Baseband Uplink Evolution



Serial RapidIO[®] Overview

Serial RapidIO is a high-performance, packet-switched, interconnect technology that addresses the embedded industry's need for:

RELIABILITY

INCREASED BANDWIDTH

FASTER BUS SPEEDS

Serial RapidIO allows chip-to-chip and board-to-board communications at performance levels scaling to ten Gbps and beyond



- C64x+™ Serial RapidIO Support – IEEE 1149.6 Compliant
 - 1.25, 2.5, 3.125 GBaud/sec per link (1.0, 2.0 and 2.5 GBits/sec w/ 8B/10B encoding)
 - Up to four 1x links (each 1x link is bidirectional) – **OR** –
 - One 4x link (bi-directional pipe), which provides up to 12.5 GBaud/sec raw
 - Up to 10Gbps for 4x link with 8B/10B encoding
 - Resulting data range 4 - 10 Gbits / sec in each direction (up to 1.25 GBytes/sec)
 - Supports DSP to DSP on the same board, DSP to Switch, etc.
- Layered architecture to minimize impact on software
- Non-proprietary multi-vendor support
- Flexible and scalable
- Reduces chip count, board area and system cost

Serial RapidIO™ Integration Advantages

•Data Flow

- “Push” or “Pull” data flow supported
- Support for Message Passing and Direct I/O
- Prioritization of data for efficient handling by DMA system

•Control

- Configurable CPU Interrupt control, with rate-limiting
- Support for Error Management
- Support for Congestion Control

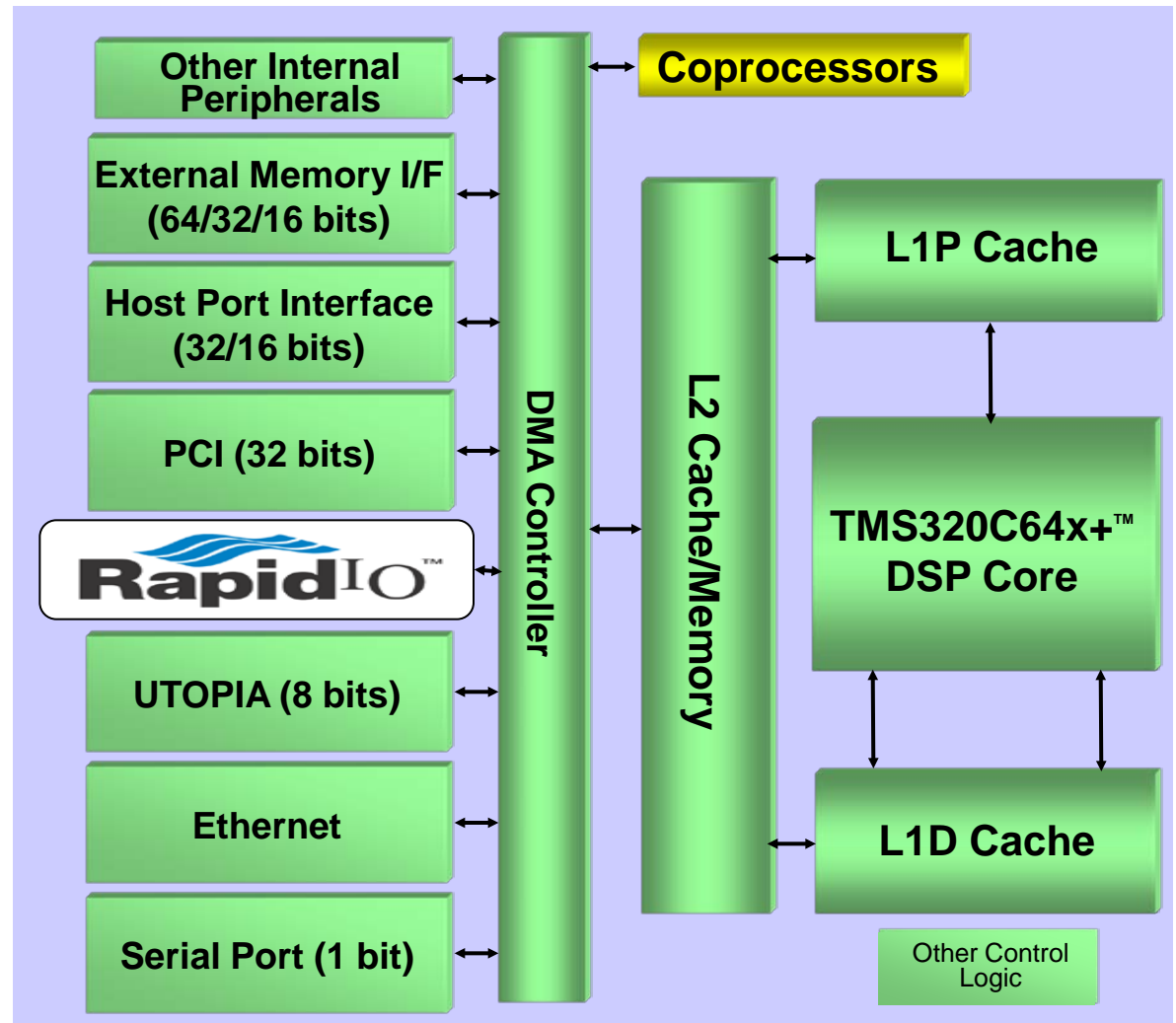
•Software Support

- Low Software overhead requires minimal CPU time
- Low level configuration and functional support

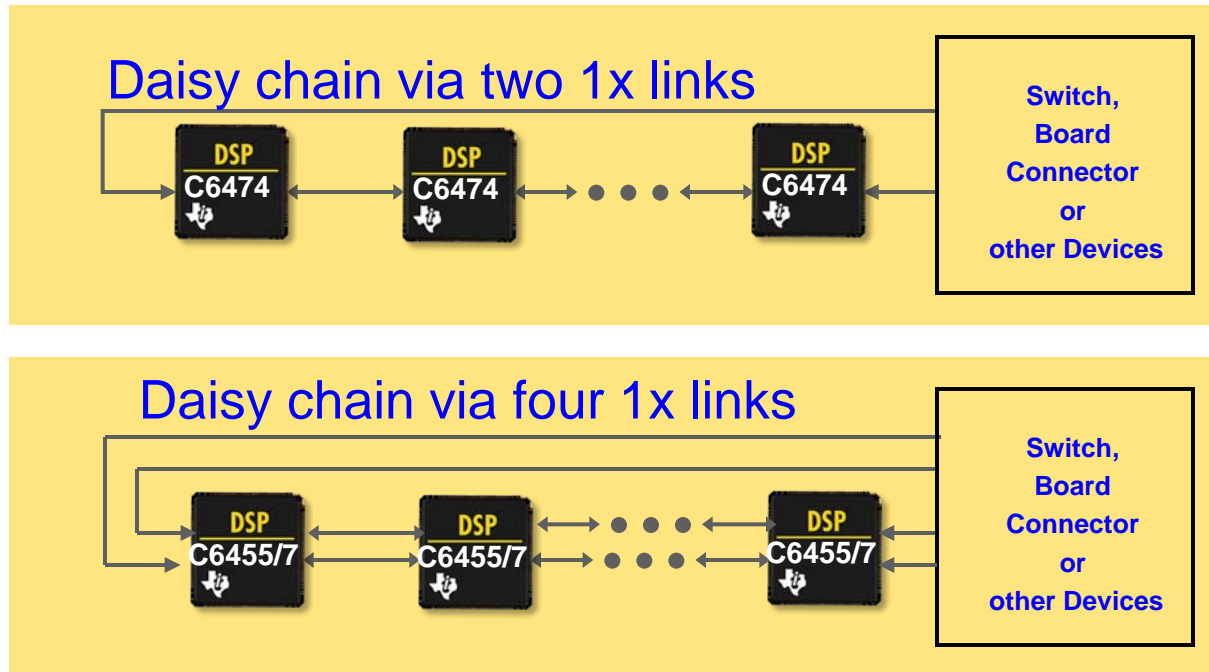
Serial RapidIO™ Integrates with DSP

Key Features

- Interfaces directly to DMA Engine
- Can queue multiple transactions
- Capable of accessing entire DSP address space

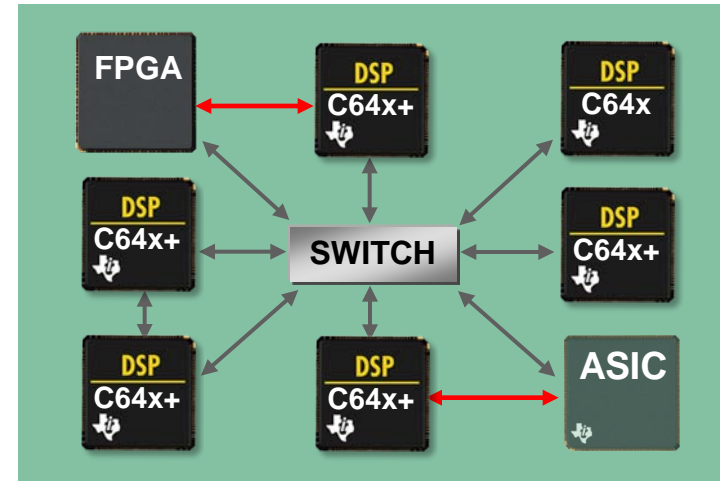
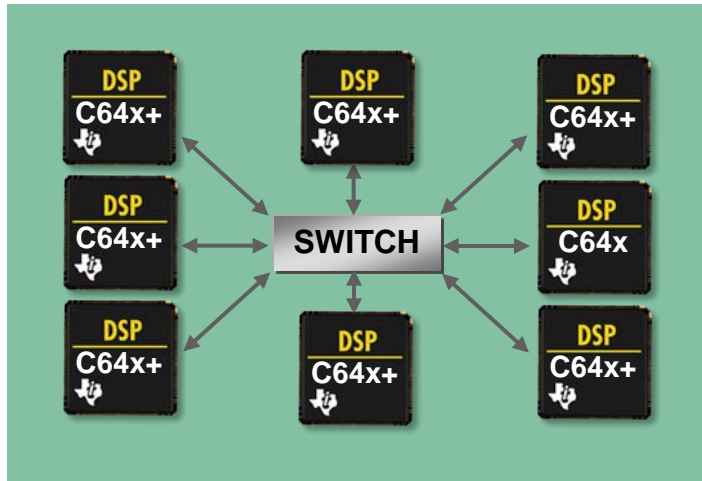


RapidIO Daisy Chain



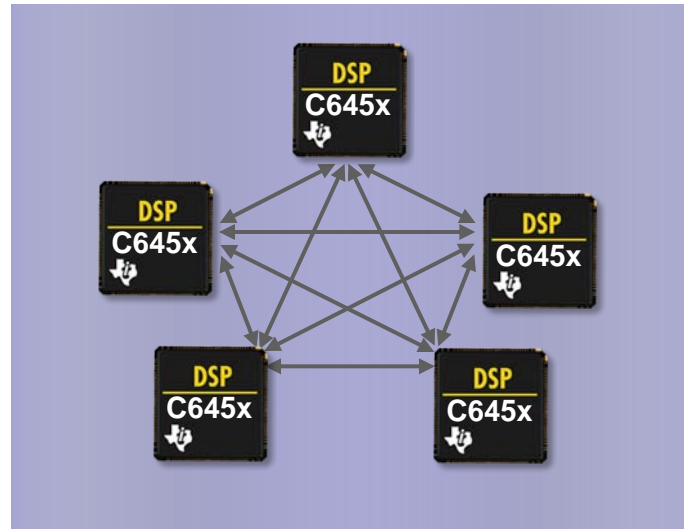
- Connect 2 / 4 lanes from DSP to DSP or other devices with RapidIO Interface
- Ideal for applications where multiple hops is acceptable
- Can be used without switch

RapidIO Switch Interconnect



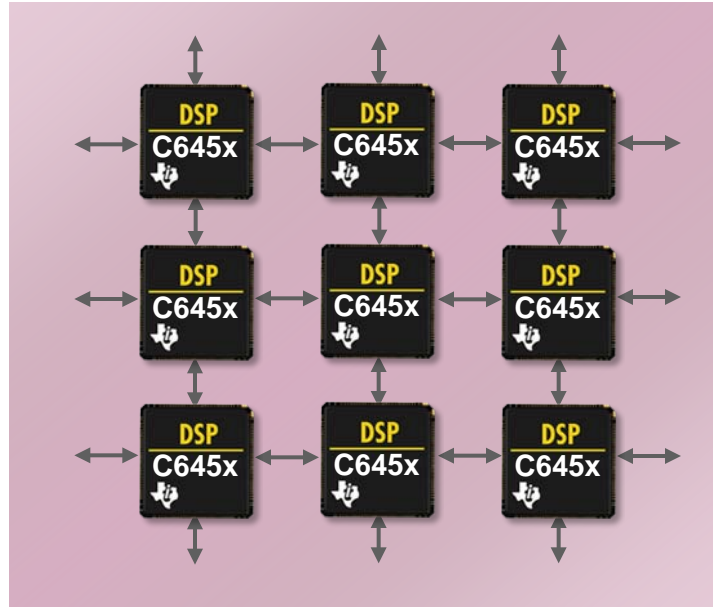
- Connect multiple DSPs to RapidIO switch via 1x or 4x lanes for DSP Farm
- For specific function where latency is critical or continuous data exchange is expected, local interconnection can be established
- Ideal where high bandwidth is needed to each device (vs daisy chain)

Direct Interconnected RapidIO



- Five DSPs are completely connected
- Provides direct connection from 1 device to any other device
- Reduces latency but limited to 1x lane bandwidth to each device

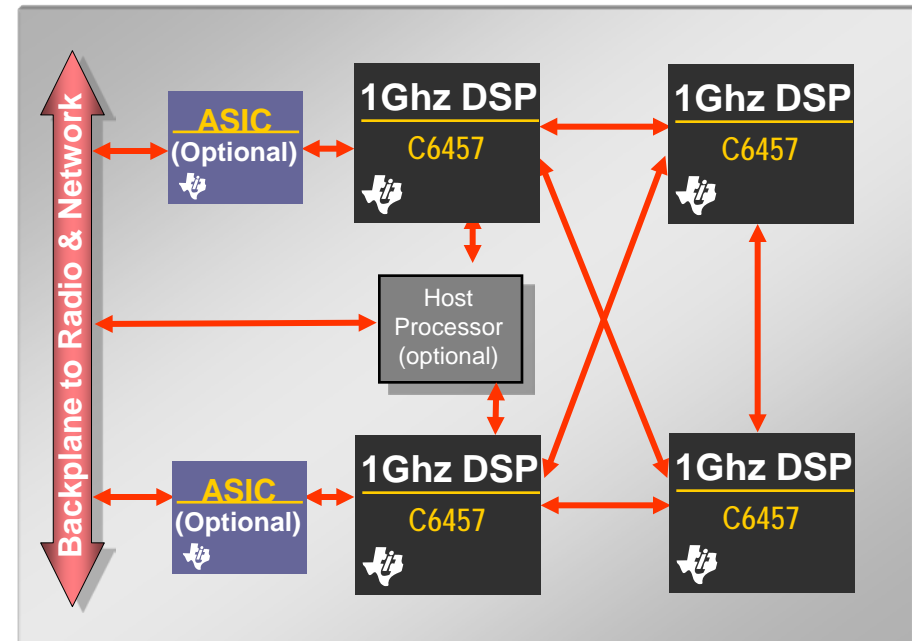
Mesh Network Configuration



- Mesh configuration with four 1x lanes
- Can be used in different mesh configurations depending upon number of RapidIO lanes available

Improved DSP Interface with RapidIO

- Direct DSP-to-DSP interconnect with optional local Host / ASIC communication
- Used in complete baseband processor card
- ASIC used for custom applications
- Based upon MAC processing needed optional HOST processor is used



TMS320C6455 DSP

Fastest Single-Core Programmable DSP Enables High-Performance Multi-Processing via Serial RapidIO® and High-Bandwidth Peripherals

Features

■ Enhanced C64x+™ Core

- 720 MHz, 850 MHz, 1 GHz, 1.2 GHz
- Up to 9600 16-bit MMACS

■ Memory

- 32 KB L1D, 32 KB L1P Cache/SRAM
- 2 MB L2, 256 K Cache/SRAM, remainder SRAM only

■ Acceleration

- Viterbi Decoder Co-Processor (VCP)
- Turbo Decoder Co-Processor (TCP)

■ Peripherals

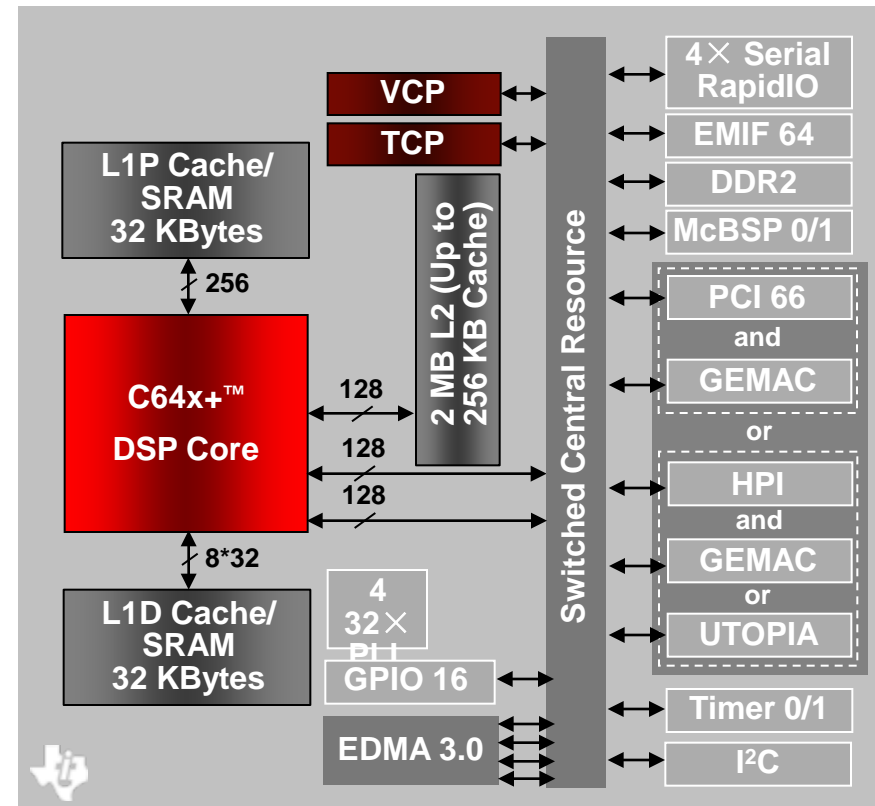
- Serial RapidIO: 10Gb/s full duplex
- Other high-bandwidth peripherals: Gigabit Ethernet MAC, UTOPIA, PCI-66, HPI
- Two EMIFs: 32-bit DDR2, 64-bit EMIF
- Package: 697 BGA, 24 × 24mm, 0.8mm, Pb-Free Balls
- Price: \$245 at 1.2GHz, \$189 at 720MHz; 10ku

Benefits

- Serial RapidIO for DSP-to-DSP, DSP-to-Switch and DSP-to-FPGA interconnectivity
- Enhanced core enables 20% higher cycle performance
- 20–30% smaller code size from 16-bit compact instructions and SPLOOP buffer

Applications

- Telecom
- Medical
- Network infrastructure
- Emerging



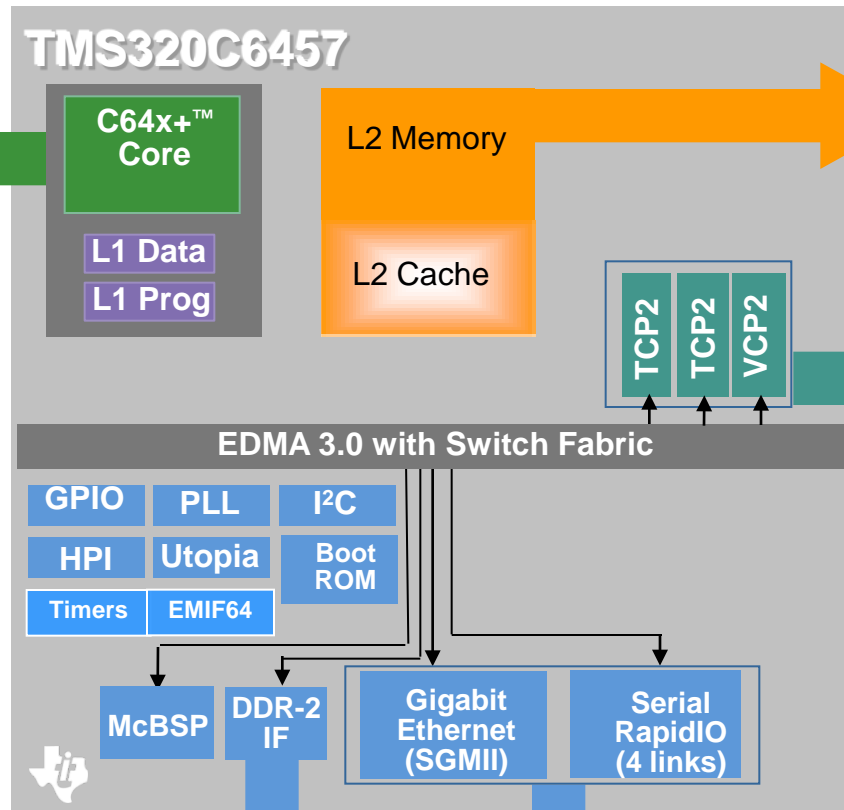
EVM Available

DSK Available

Pin compatible
with C6454 DSP

TMS320C6457 high performance DSP

- 1.2 GHz DSP delivers 9,600 (16-bit) MMACS peak
- Based on TI's flagship C64x+ DSP core (achieved BDTI's highest speed score)
- 100% backward compatibility with other C64xx DSPs enables legacy code re-use for development efficiency & faster time-to-market.
- 65nm process
- ~4 Watts (preliminary estimate; power characterization not yet completed)
- 23mm x 23mm



- 2 MB of L2 memory
- Up to 1 MB L2 cache (4X improvement)
- Enhanced memory & cache architecture improves performance

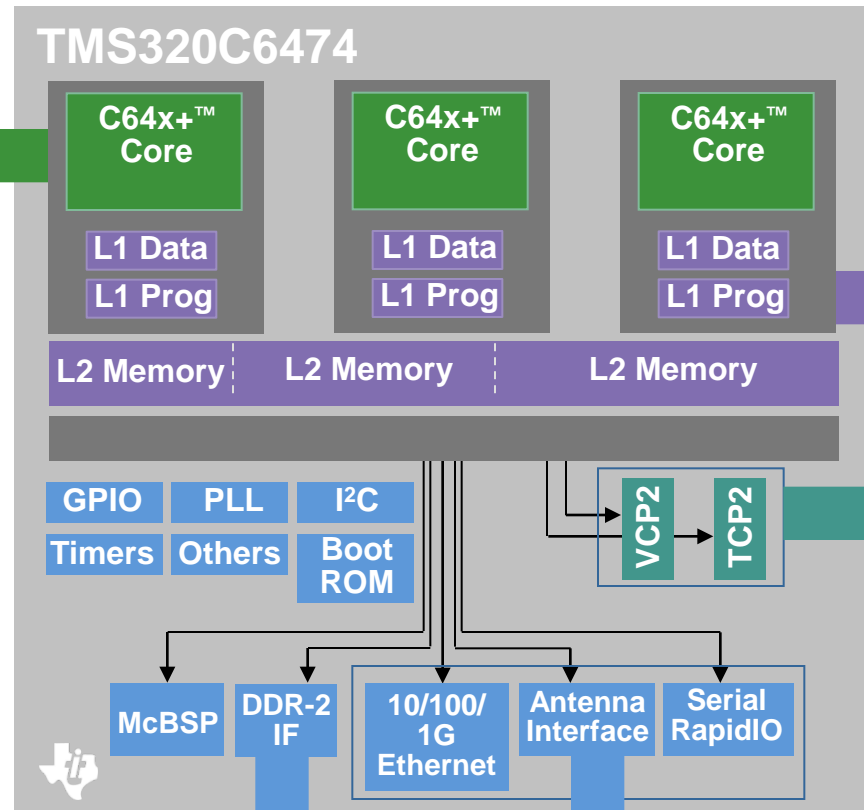
- Two TCP2 (2x improvement) & one VCP2 telecom accelerators for significant speed up of channel decoding operations on-chip to offload the C64x+ core

- Access memory faster with TI's fastest 667 MHz DDR-2 interface on any DSP (25% improvement)

- High-speed interconnect enabled by Serial RapidIO & Gigabit Ethernet MAC SERDES interfaces

Customers achieve greater performance density with three 1 GHz cores on a single chip

- Three 1 GHz cores, 48,000 (8-bit) MMACS / 24,000 (16-bit) MMACS peak performance
- Software backward compatibility allows for easier porting to new DSP
- Fast core-to-core communications, less cycles/lower latency



- 3 MB total L2 memory
- Configurable allocation per core

- VCP2 and TCP2 accelerators for significantly speeding up channel decoding operations on-chip, offloading the DSP for other processing

- Access memory faster with 667 MHz high performance DDR-2

- High-speed interconnect enabled by EMAC, AIF and SRIO SERDES interfaces

TI's commitment to RapidIO 2.0

- TI has signed agreements with IDT to license their RapidIO Gen 2 IP.
- TI will utilize this new IP in next generation DSPs for wireless infrastructure and mass market segments
- Guarantee interoperability with IDT RapidIO switches

Summary & Conclusion

- High performance DSP requires high data throughput serial interconnect
 - **Driven by need for low pin count, large data exchange and bandwidth scalability**
- For embedded system applications, serial RapidIO is the best technical choice
 - **Peer to Peer Connectivity & Switch Fabric Capability**
 - **Performance/Flexibility**
 - **Support of embedded players**
 - **Rich choice of speeds and widths**
- RapidIO has gained momentum with silicon vendors and end equipment manufacturers.
- TI is committed to support serial RapidIO in all high performance DSPs
 - **TI made the first DSP with Serial RapidIO.**
 - **RapidIO is strategic to TI high performance DSP roadmap.**
 - **TI promise to support RapidIO v2.x on DSP.**

Q&A