



# **Xilinx Serial RapidIO Solution in**

## **Virtex 6/ Spartan 6 High Performance Low Cost FPGA Technology Platforms**

**RapidIO Trade Association Summits  
Oct 2009**

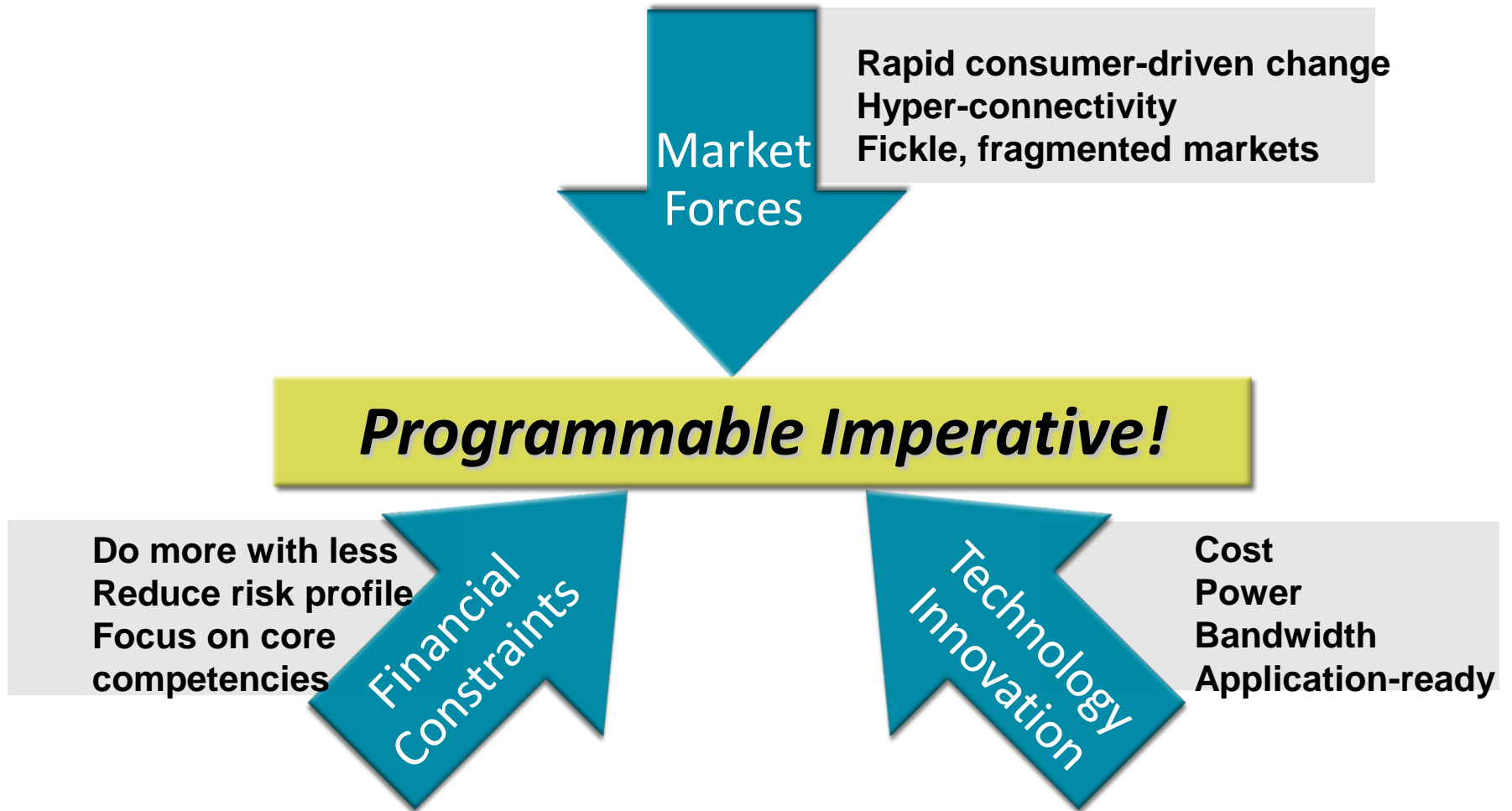
# Topics

- **Xilinx FPGA Technology**
- **Xilinx Serial RapidIO IP**
  - Value Proposition
  - Features/ Functions
  - Usage Models
  - Others
- **Summary**

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# Xilinx FPGA Technology



***Xilinx FPGA technology advances address market & technology challenges***

# Xilinx Virtex-6 and Spartan-6 FPGA Families

Up to **60%** lower system cost

Up to **65%** power reduction

Up to **50%** development time reduction

Over **1Tbps** IO bandwidth

**Breakthrough performance, lower power, and lower cost pushing programmability beyond the tipping point**



# Virtex-6 and Spartan-6 FPGAs

## Addressing the Broad Range of Technical Requirements

**Virtex-6  
LXT**



- High Logic Density
- High Speed Serial Connectivity

**Virtex-6  
SXT**



- High Logic Density
- High Speed Serial Connectivity
- **Enhanced DSP**

**Virtex-6  
HXT**



- High Logic Density
- **Ultra-high Speed Serial Connectivity**

**Spartan-6  
LX**

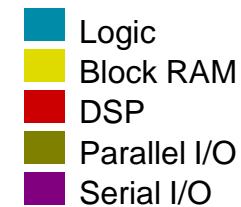


- **Lowest Cost Logic**

**Spartan-6  
LXT**

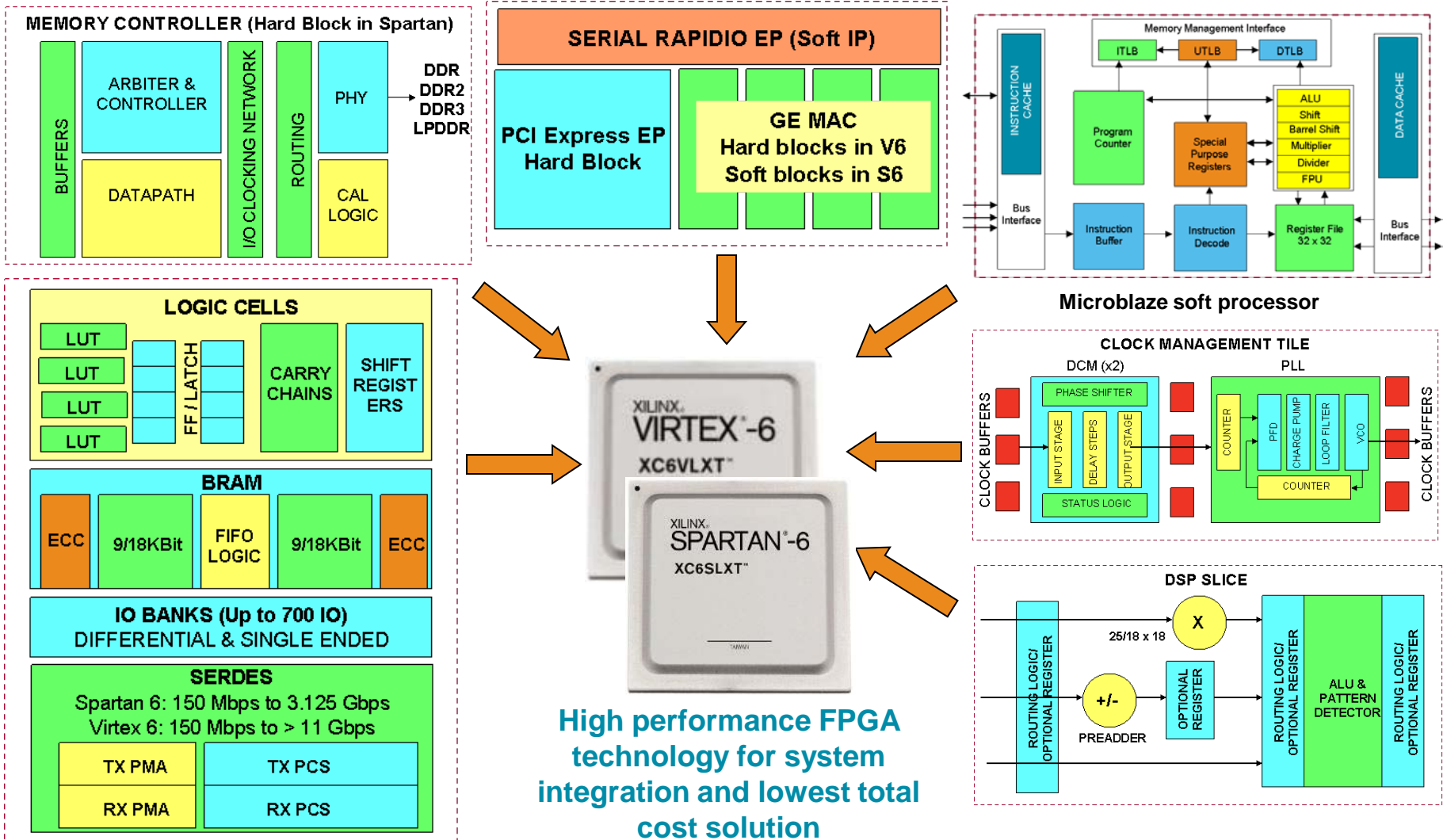


- **Lowest Cost Logic**
- **Low Cost Serial Connectivity**



# Xilinx FPGA Technology Platforms

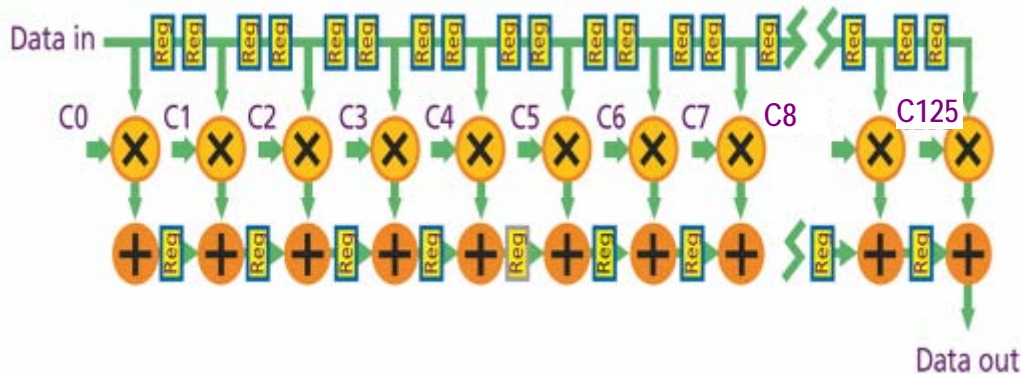
## Xilinx Virtex-6 / Spartan-6 FPGA Architecture



# FPGA DSP Compute Advantage

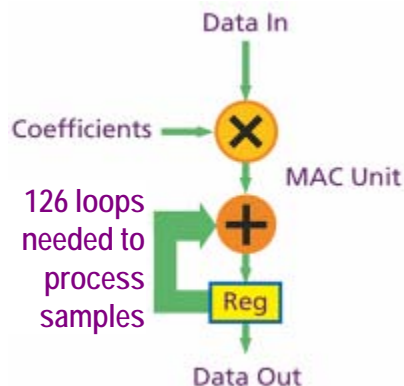
*Capacity to deliver much higher DSP performance*

## FPGA-based DSP - Parallelism



$\frac{550 \text{ MHz}}{1 \text{ clock cycle}} = 550 \text{ MSPS}$	<b>Virtex-DSP</b> X5 filters
$\frac{250 \text{ MHz}}{1 \text{ clock cycle}} = 250 \text{ MSPS}$	<b>Spartan-DSP</b>

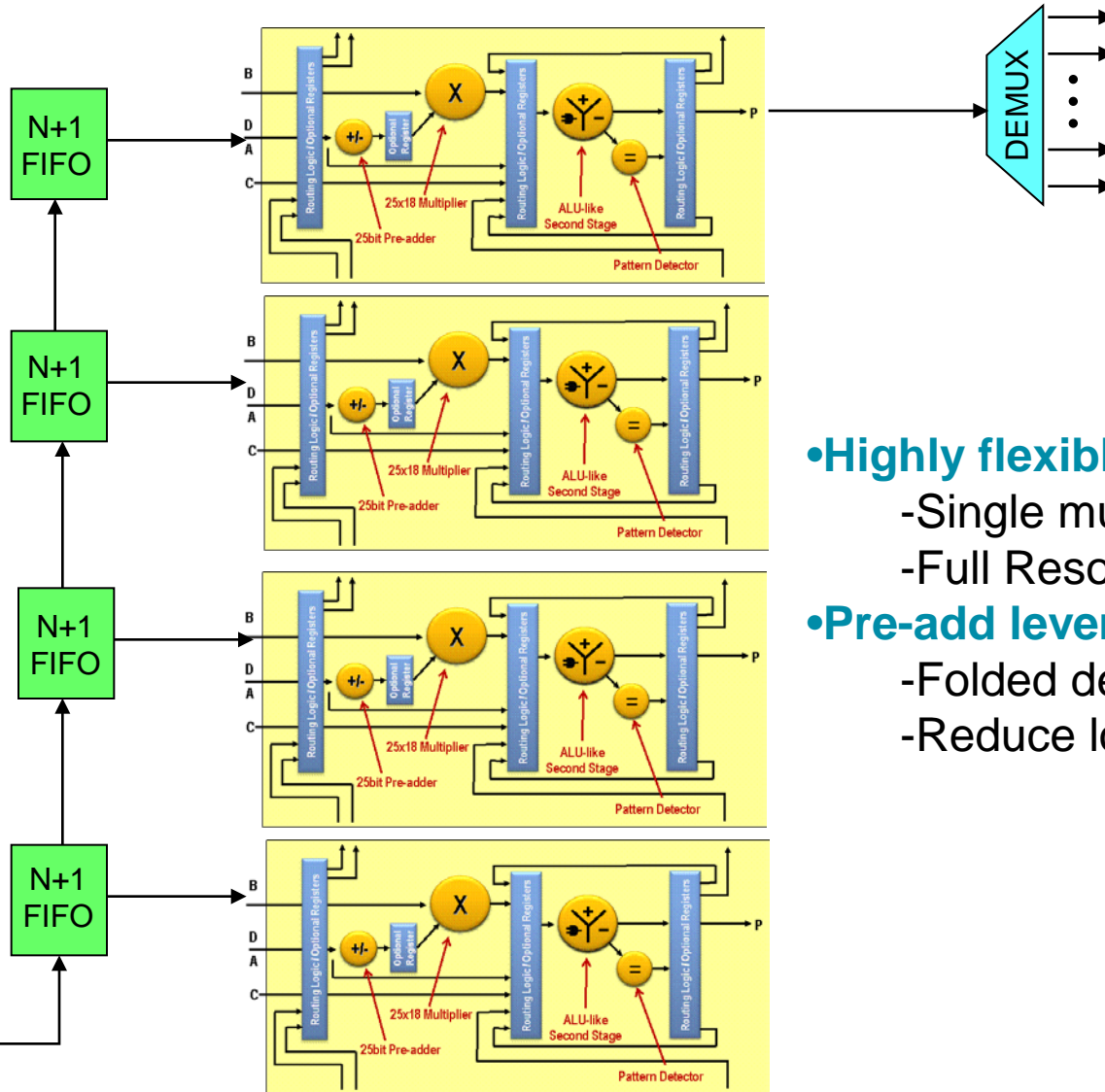
## Conventional DSP Processor - Serial



$\frac{1 \text{ GHz}}{126 \text{ clock cycles}} = 8 \text{ MSPS / MAC unit}$
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# Parallel DSP Processing in Virtex 6

## Multi-channel FIR Filter Example Design



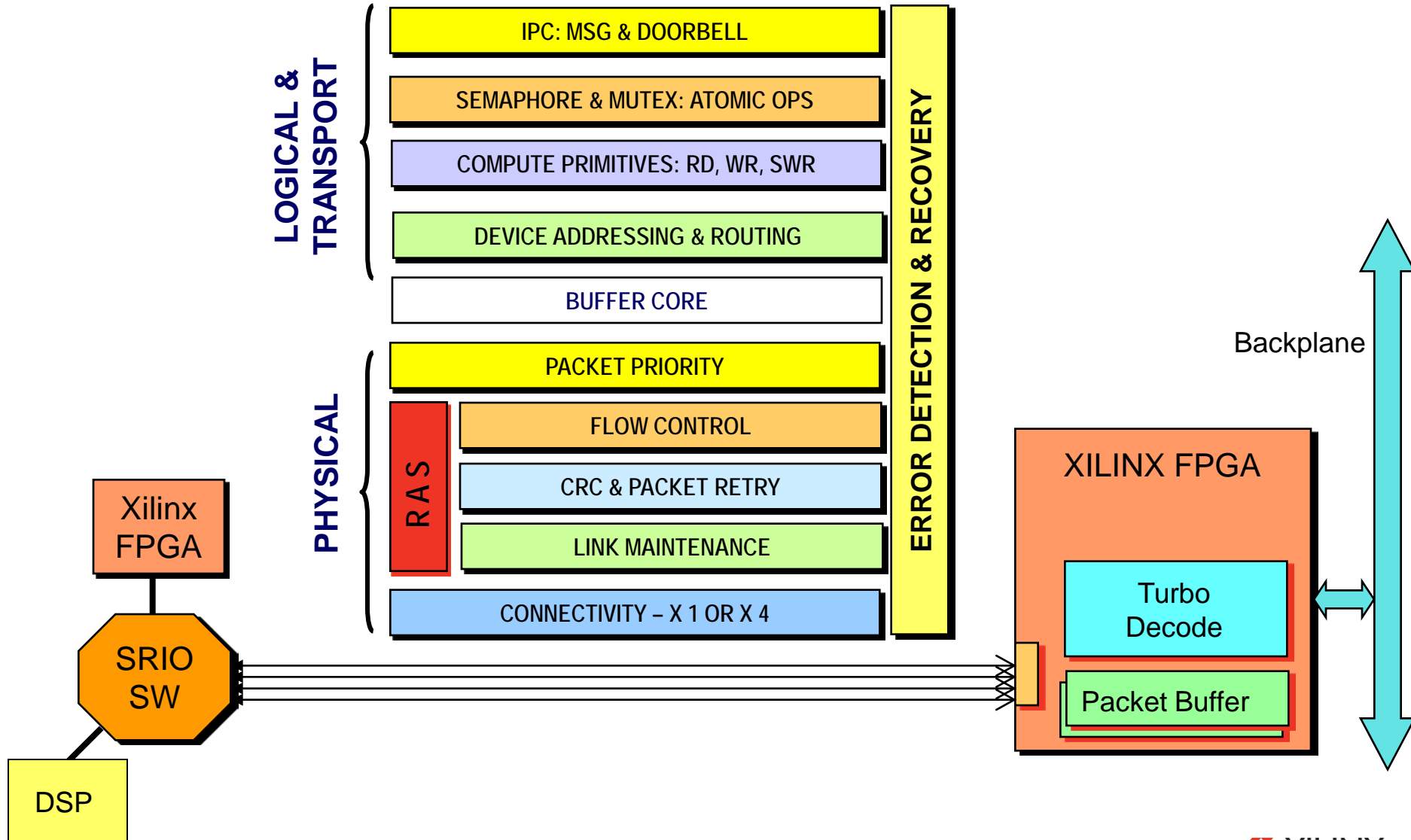
- **Highly flexible DSP slice architecture**
  - Single multiplier per slice
  - Full Resource utilization
- **Pre-add leverages filter symmetry**
  - Folded design to reduce size
  - Reduce logic, routing & power

# Topics

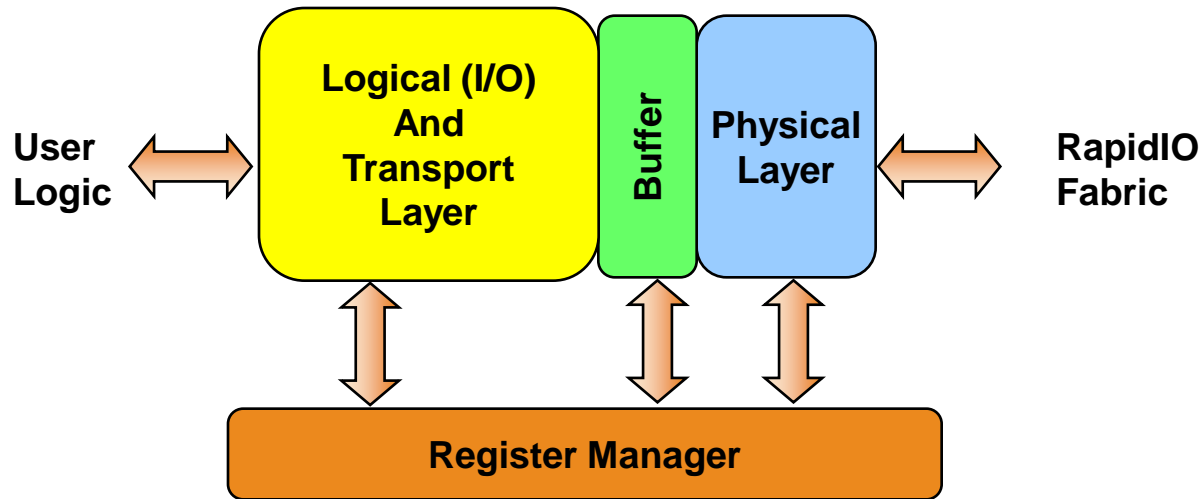
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# Serial RapidIO Protocol Overview

*Not Just a Connectivity*



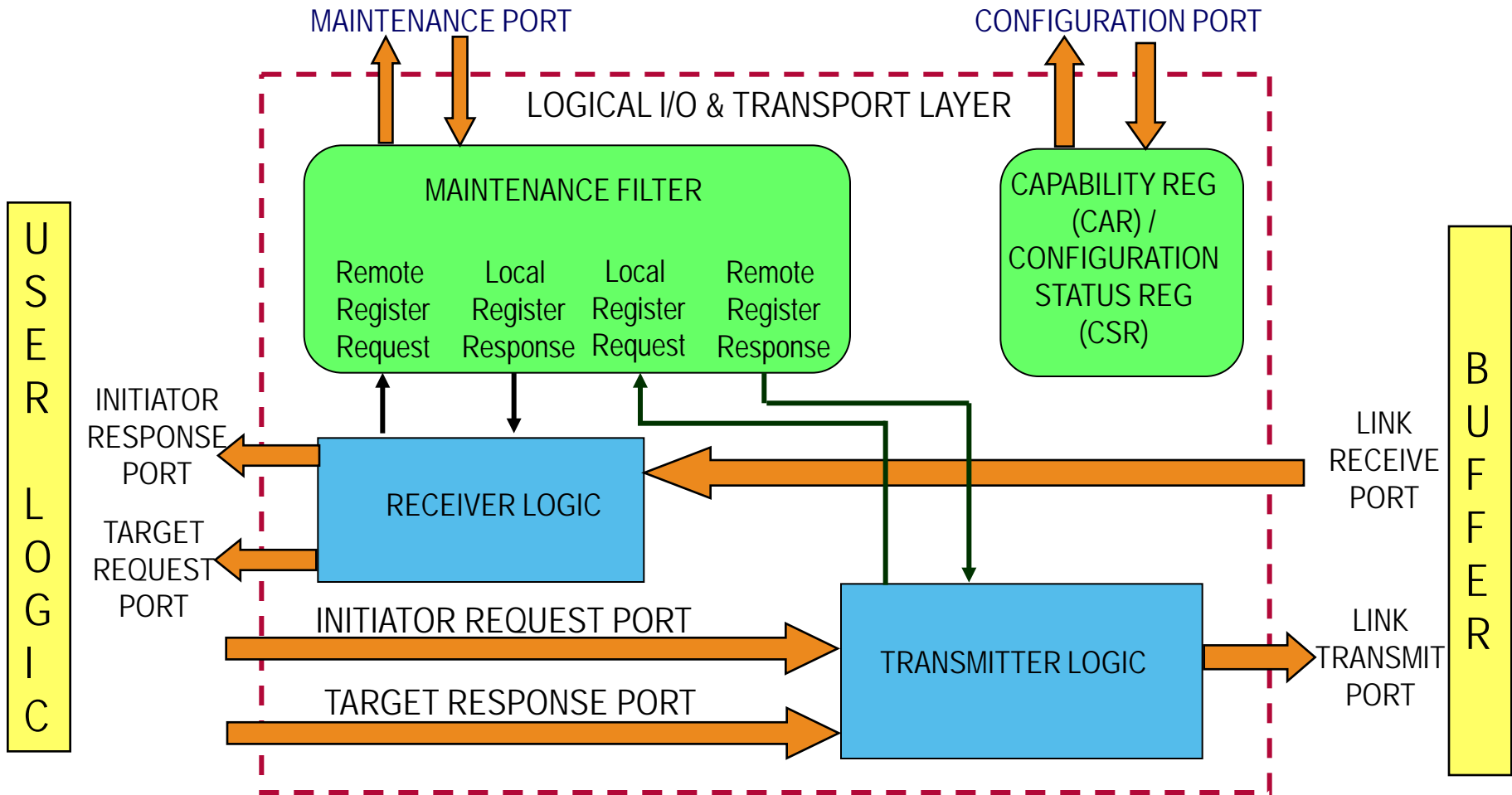
# Xilinx Serial RapidIO IP



## ▪ **Serial RapidIO PHY and Logical IO & Transport LogiCORE**

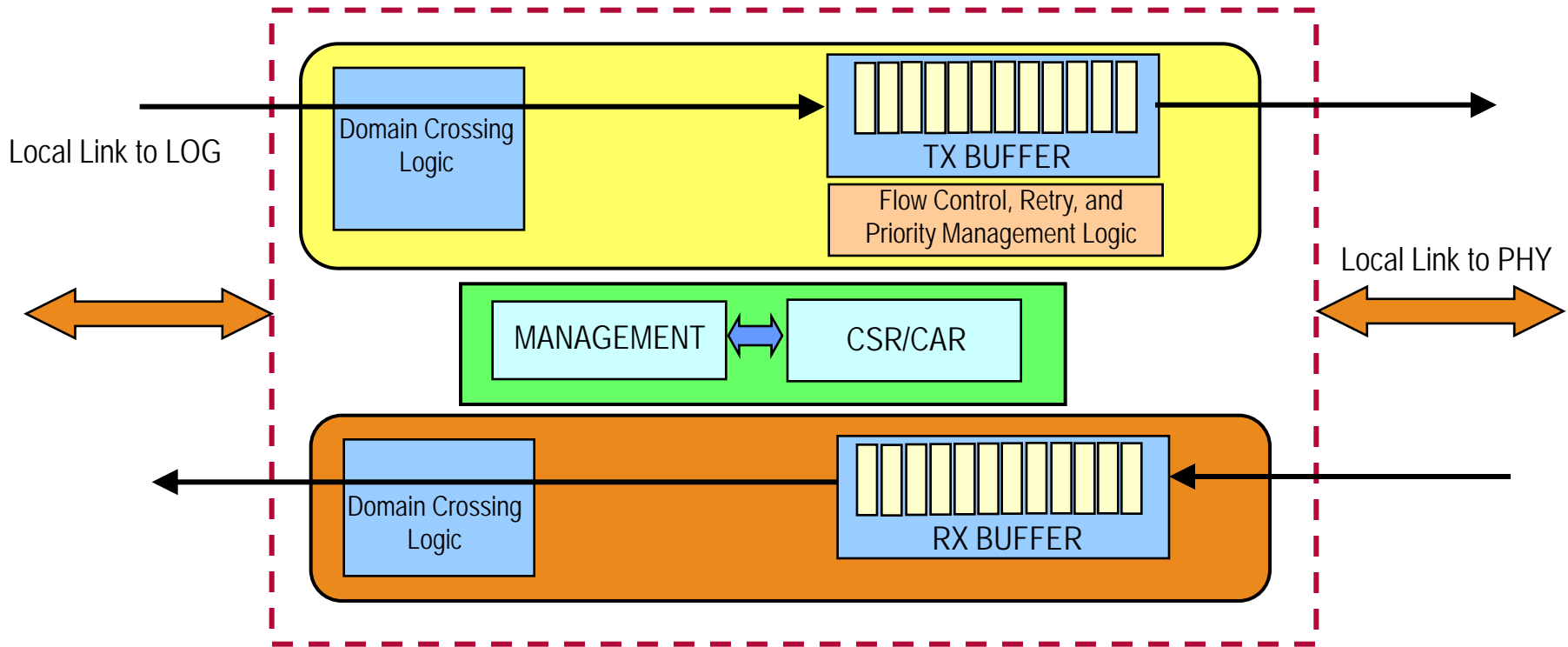
- Supported on Virtex V6, V5, V4, and Spartan S6 Silicon Platforms
- Serial RapidIO Version 1.3 Specification compliant
- Line speeds of 1.25, 2.5, 3.125 Gbps for x1 and x4 Link Width
- Configurable & optimized Buffer Core
- Compliant to RIOLAB level I, level II, and level III certification

# Logical I/O and Transport Layer



Logical I/O and Transport Layer LogiCORE provides SRIO transaction specific ports to ease User Application design

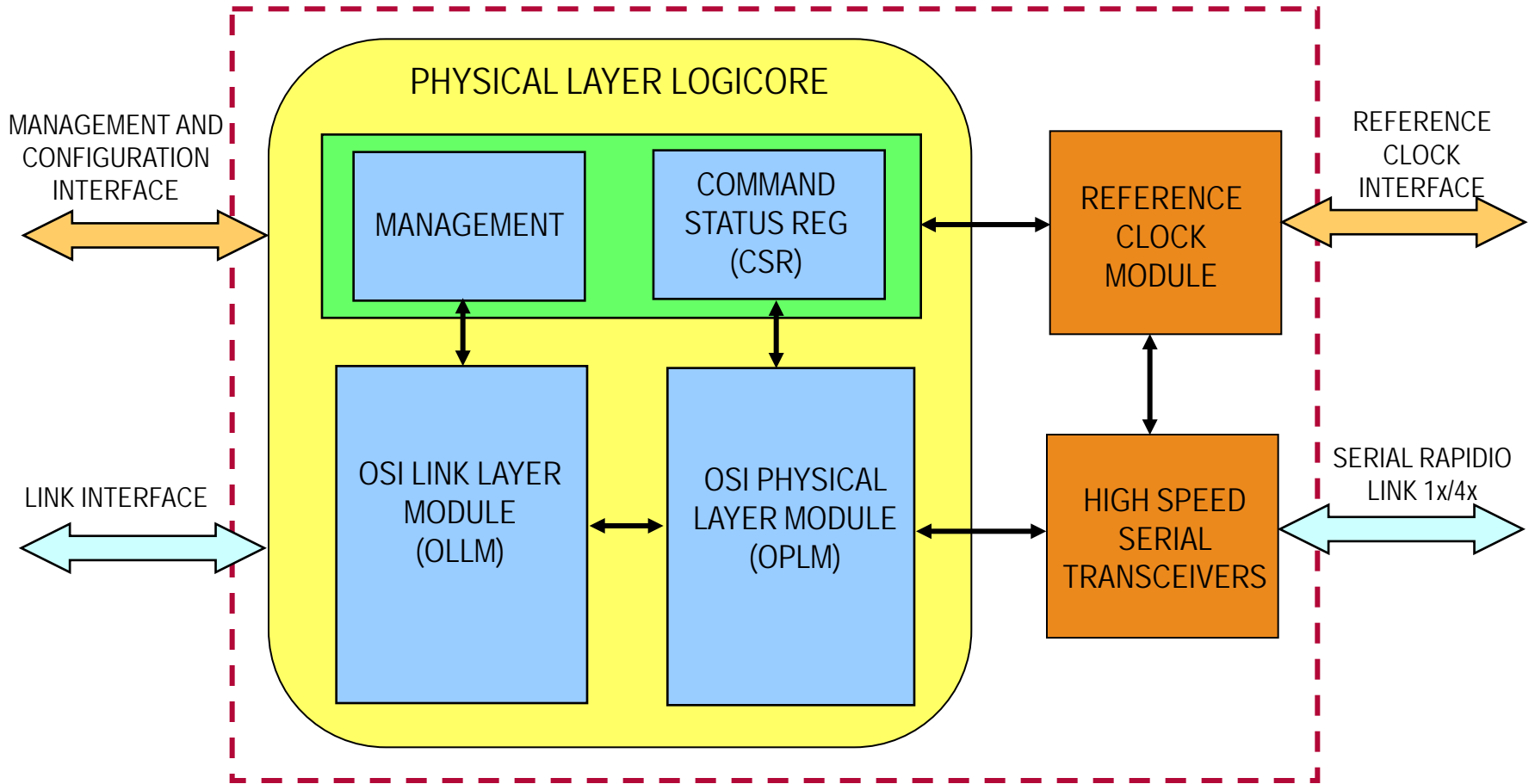
# Buffer Core



## Buffer Core – Flexible & Optimal

- Configurable Buffer (8, 16, or 32 packets)
- Flow Control & Priority Management – *supports both RX & TX Flow Control*

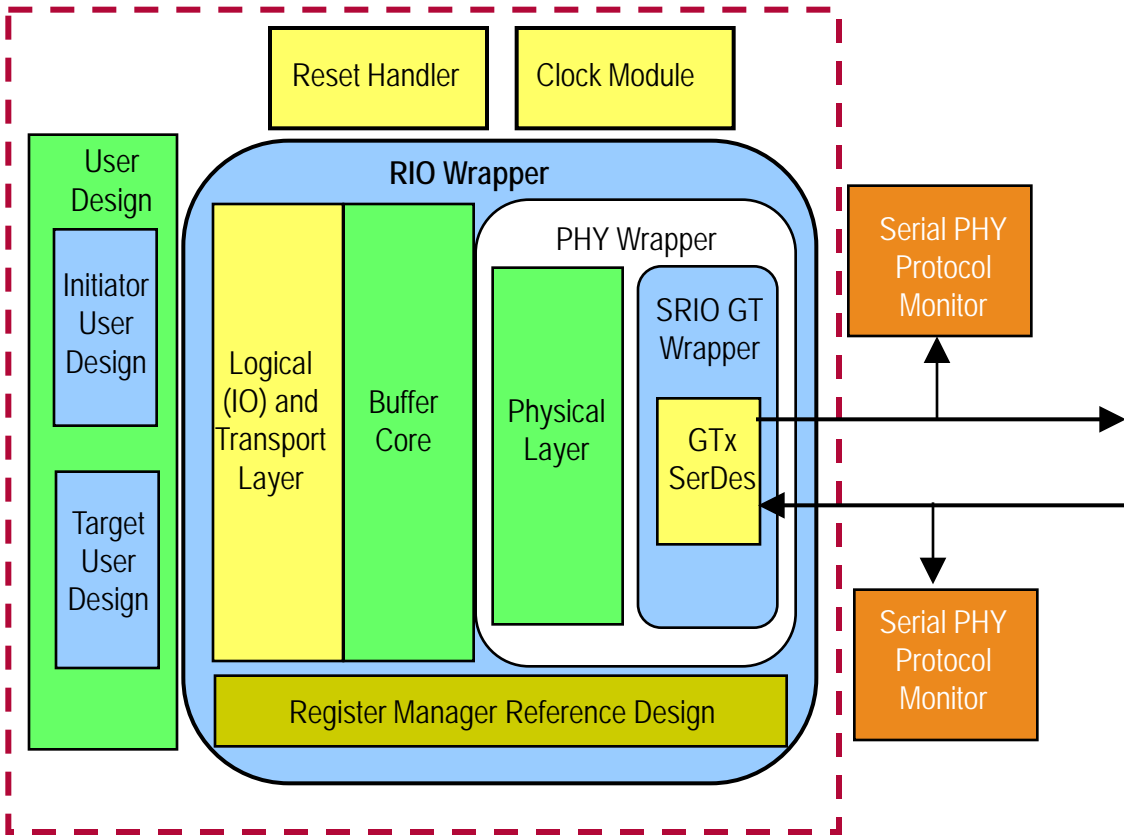
# Physical Layer LogiCORE



Xilinx SRIO PHY LogiCORE has flexible link interface to allow simple & optimal connectivity to Packet Buffer

# Xilinx Serial RapidIO Endpoint

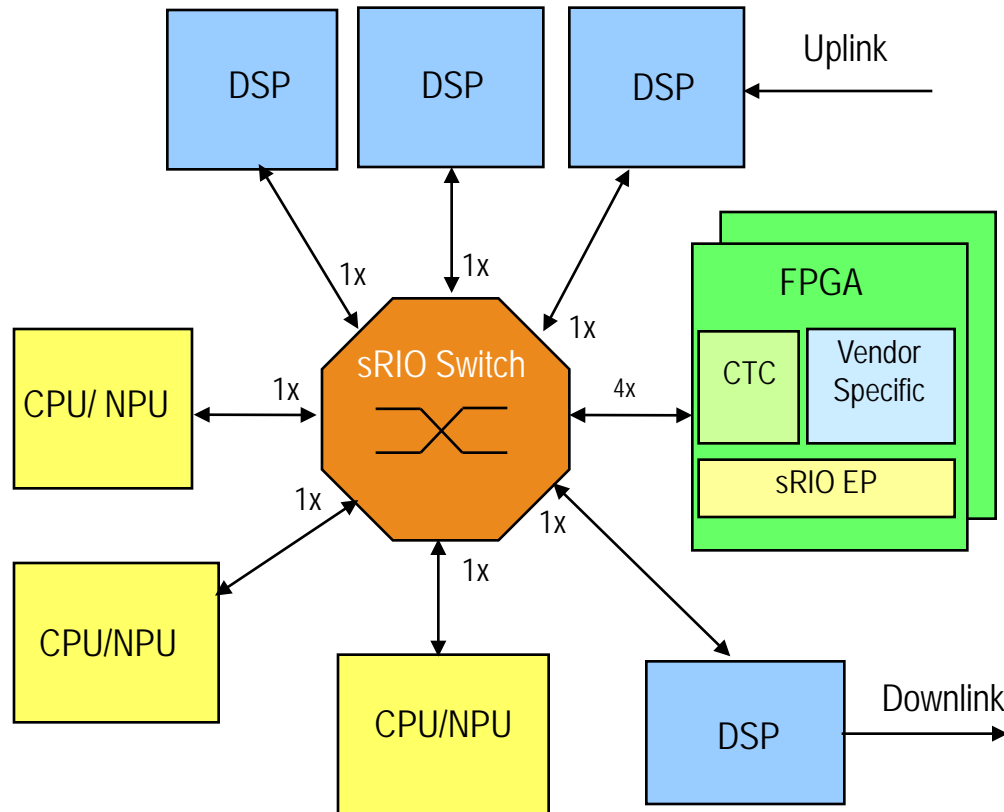
## Example Design



SRIO EP example design is provided with the core that implement simple target/ Initiator User design

# Usage Models – DSP/FPGA Farms

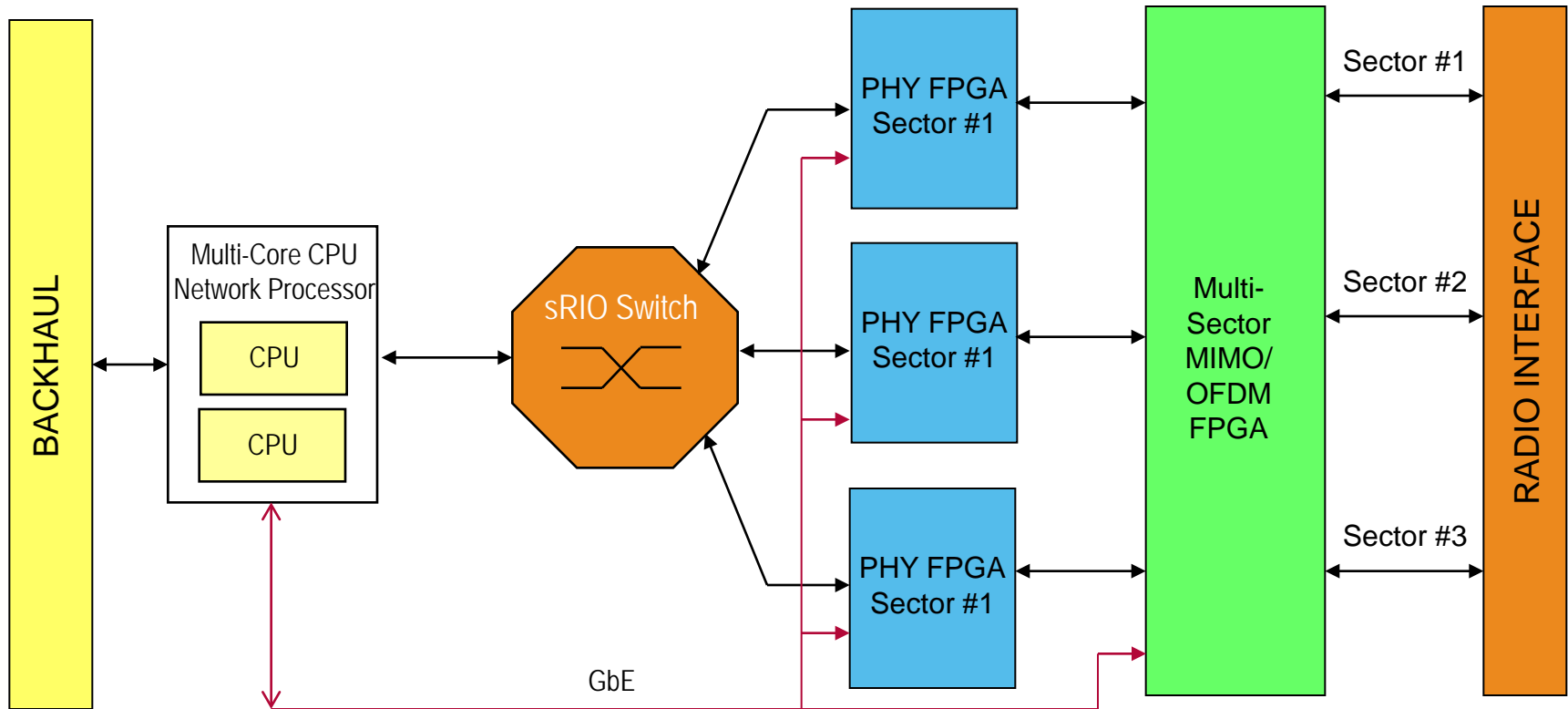
## Channel Card traditional Architecture



**Function based architecture has higher latency due to Multiple hops and needs more processing horsepower**

# Channel Card Architectural shift

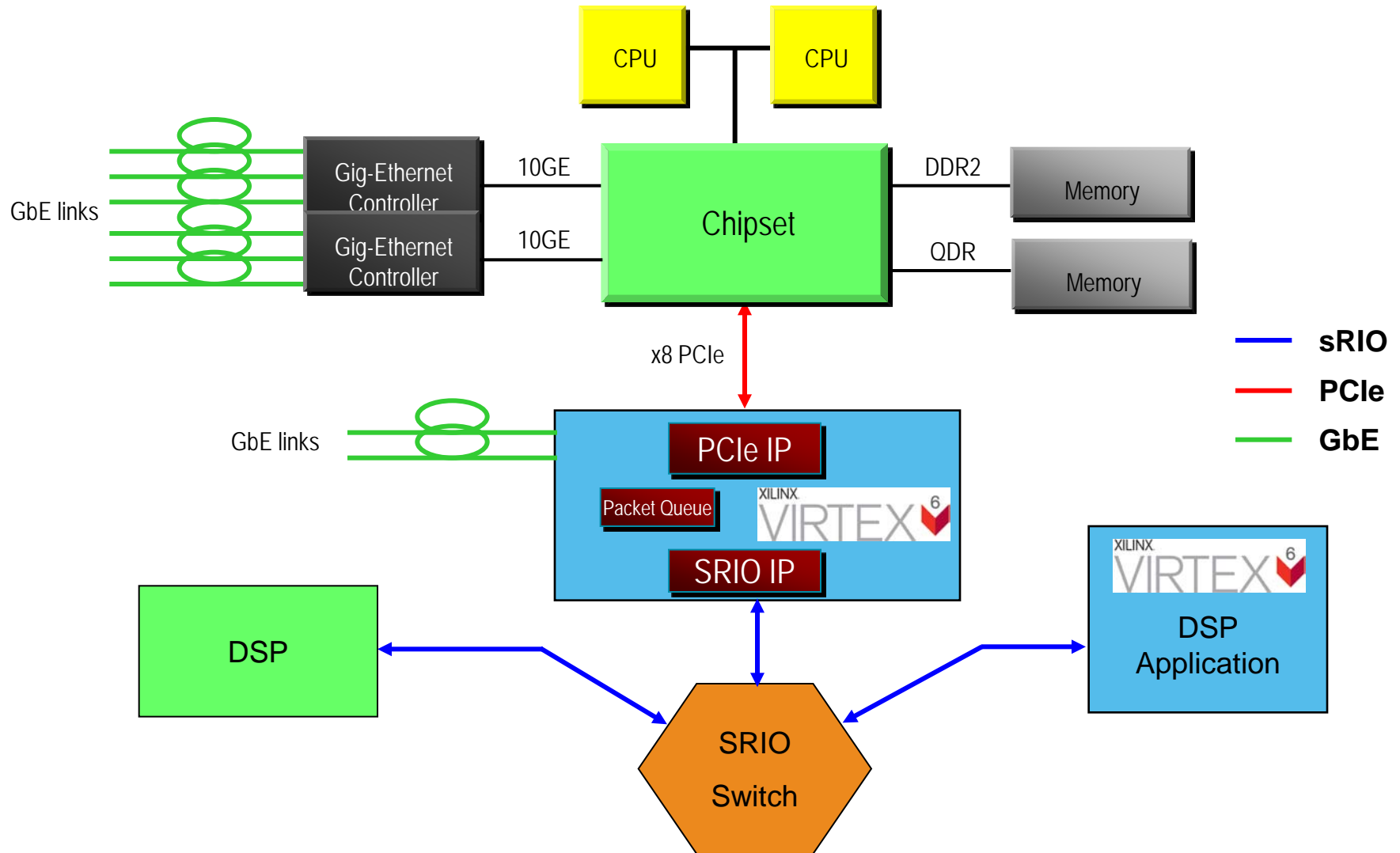
## *Sector Based Architecture*



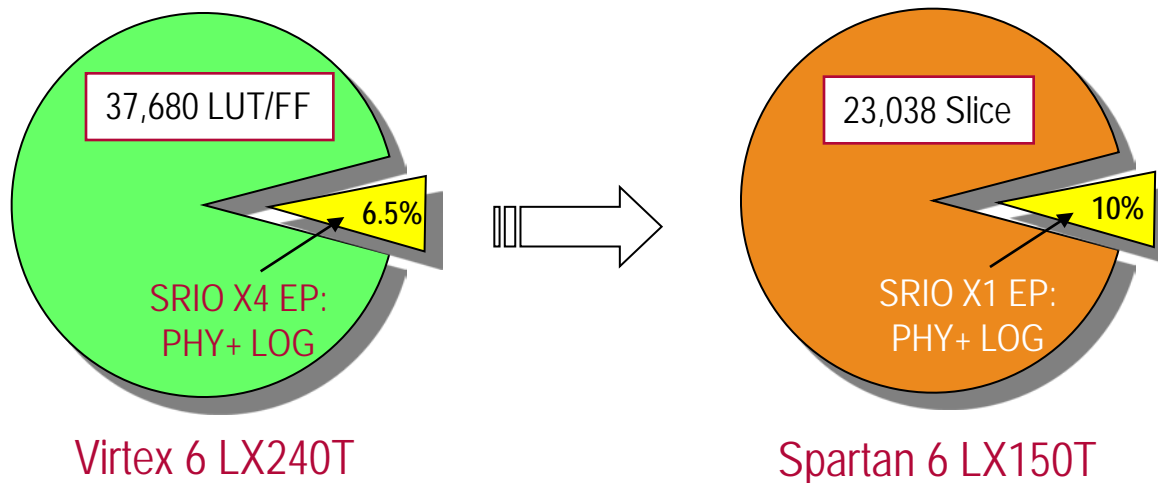
**Sector based architecture is scalable and reduces bandwidth requirements and switching cost**

# Embedded Systems

## Typical Use Case - Bridging



# Xilinx SRIO EP IP Size

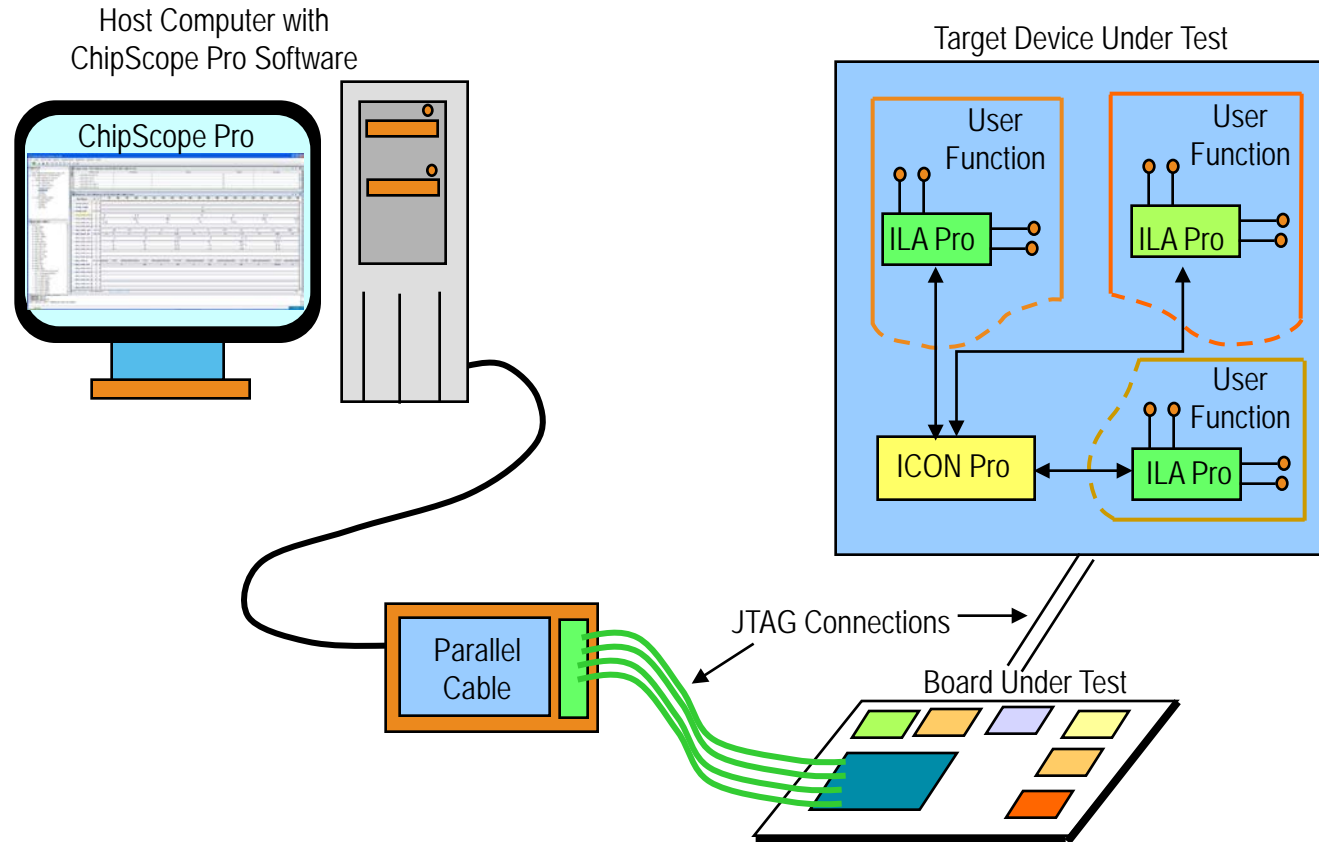


Buffer Core takes additional 500-700 LUTs

	Virtex 6		Spartan 6
SRIO PHY	x1	x4	x1
LUT	3450	3950	3100
FF	2650	3250	2650
SRIO LOG			
LUT	1850		1800
FF	1800		1800

# Xilinx ChipScope Pro Tools

## On-Chip Debug



Xilinx ChipScope Pro is an integrated part of the Xilinx design flow that can be easily instantiated to reduce debug & verification time

# Xilinx Chipscope Pro + IBERT

## Eye Scan Feature for Transceiver Debug

**IBERT Console - DEV:1 MyDevice1 (XC5VLX50T) UNIT:0 MyIBERT1**

MGT/BERT Settings | DRP Settings | Port Settings | Sweep Test

MGT118\_0 | MGT118\_1 | MGT120\_0 | MGT120\_1

Set Sweep Params to Current MGT Values | Clear All | Log File Settings

Parameter Settings

Parameter Name	Start Value	End Value	# of Values
TX Diff Swing	800 mV	1100 mV	3
TX Pre-Emphasis	0%	12%	4
RX Eq	Off	Off	1
TXRX_INVERT	000	111	8
HMA_RX_CHG	9-0030	9F00E+	16
RX Sampling Point	47	52	1

Ad./Remove Ports/All ibules

Total Iterations: 1536 | Current Iteration: 1 | Time Per Iteration (s): 1

Status/Results

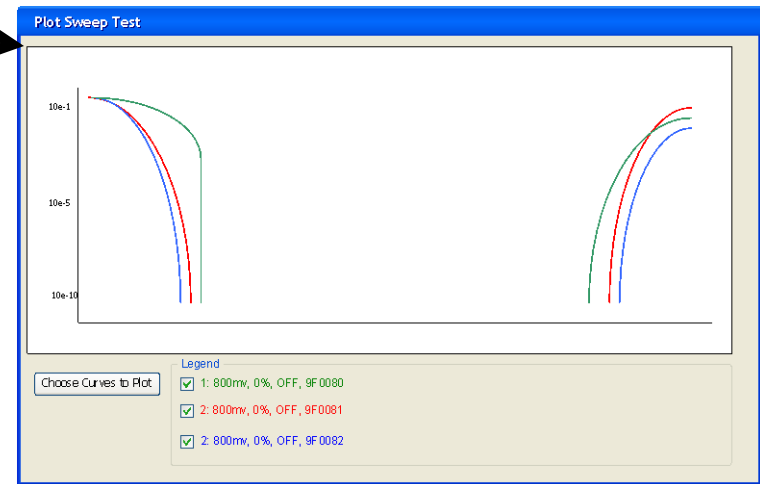
Start | Pause | Reset | Plot

TX Diff Output Swing = 800 mV (Port TXDIFFCTRL0[2:1] = 000, Port TXDIFFCTRL0[2:0] = 000);  
 TX Pre-Emphasis = 0% (Port TXPREEMPHASIS0[2:0] = 000);  
 RX EQ Enable = 0% (Port RXEQEN0 = 1);  
 TXRX\_INVERT = 000;  
 HMA\_RX\_CHG = 9F00E+

**Eye Sweep (ps)**

RX Sampling Point

- Can move sampling point within the eye opening horizontally
  - Support for vertical scan coming soon
- Can measure jitter margin vs. Bit Error Rate for a particular channel and Equalization setting
- Can sweep Equalization settings to find optimal setting
- Allows easy Channel Margin Analysis



**Ideal Sampler Position**

# Summary

- **Xilinx FPGA Silicon Architecture advances address market and technology challenges**
  - Ideal system integration platform with high performance DSP & compute logic and connectivity at low cost and power
  - Allows flexible & scalable system design to address rapidly changing requirements in increasingly fragmented markets
- **Xilinx Serial RapidIO**
  - Most widely deployed and time tested soft IP
  - Optimal: High throughput and small footprint
  - Flexible & scalable architecture
  - Internally developed and supported