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The Standardized 3G Base Station

TUNDRA

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Overview

- Downward Migration of Standardization
- Switched Baseband Architecture
- Conclusions

Cost Pressures

- Node B represents a significant portion of infrastructure cost to achieve requirements for coverage and capacity
- 3GPP standardization stops at the boundary of the Node B
- Other standardization efforts are creating standard interfaces within the Node B:
  - Common Public Radio Interface (CPRI)
  - Open Base Station Architecture Initiative (OBSAI)
- These “intra-Node B” standards create opportunity for more cost-effective Node B development and supply

Processing Standardization

- Another “standardization” opportunity concerns chip rate processing
- Chip Rate includes correlation, channel estimation, multi-user detection. Chip rate is particularly intensive for uplink (reverse) direction
- Symbol Rate includes de-interleaving, Viterbi decoding (voice) and Turbo decoding (data)
- Chip rate traditionally processed with ASIC or FPGA solutions (may be some DSP-assist in uplink direction)
- Symbol rate with DSP
- There is a significant value proposition in software chip rate processing to allow for different traffic patterns
- Software chip rate processing solutions are here and more will arrive over time

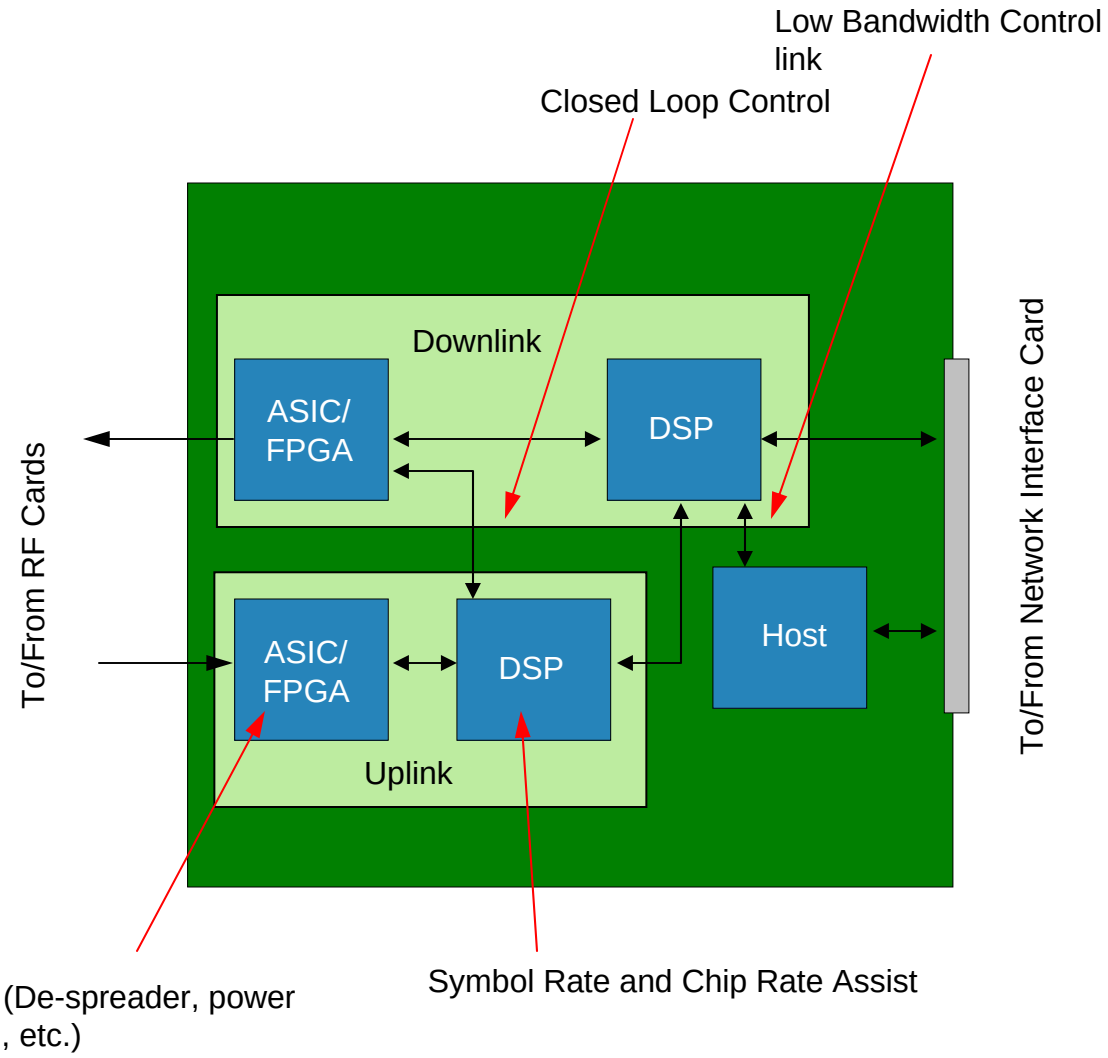
Pressures for S/W Approach

- Initial Node B installations for coverage and mostly voice
- Next generation designs to increase capacity and more data
- Usage (voice vs data) is difficult to predict
- Interference cancellation and beam-forming will be more important for capacity. Approaches are not finalized
- Fixed hardware approaches will give way to more flexible software approaches

Fixed Approach

Baseband Processing

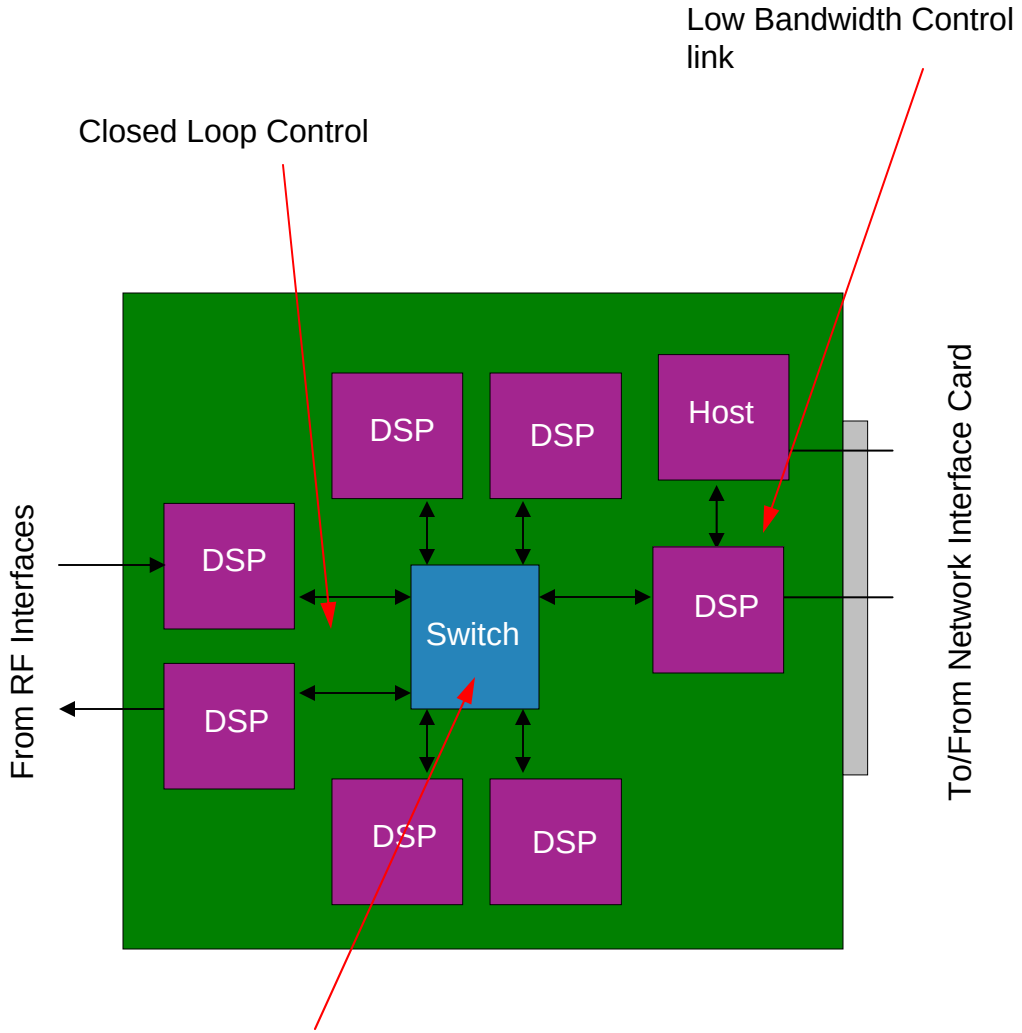
- **DSP in Uplink direction typically adds chip rate "assist" functions**
- **Closed Loop Control important for low latency power control feedback**
- **ASIC/FPGA may be shared between Uplink/Downlink**
- **Links to/from RF cards typically proprietary LVDS**
- **No Peer-to-Peer requirement**
- **2G/2.5G or new 3G, fixed voice/data assumptions**



Flexible Approach

Baseband Processing

- **Much higher complexity requirements (e.g. Multi-User Detection)**
- **Blurred lines between Chip Rate and Symbol Rate**
- **More Peer-to-Peer communication**
- **Higher throughput and more dynamic environment (e.g. voice vs data)**



Chip Rate and Symbol Rate Algorithms load balanced amongst DSPs

Interconnect Standardization

- Programmable chip rate processing entities are a good thing, but would also need to be interconnected a certain way to enable their inherent flexibility
- Interconnect needs to support high bandwidth, low latency bi-directional traffic
- Would ideally be hardware terminated so DSPs are not handling protocol stack of interconnect
- This places constraints on how processing elements are connected to antenna and to each other

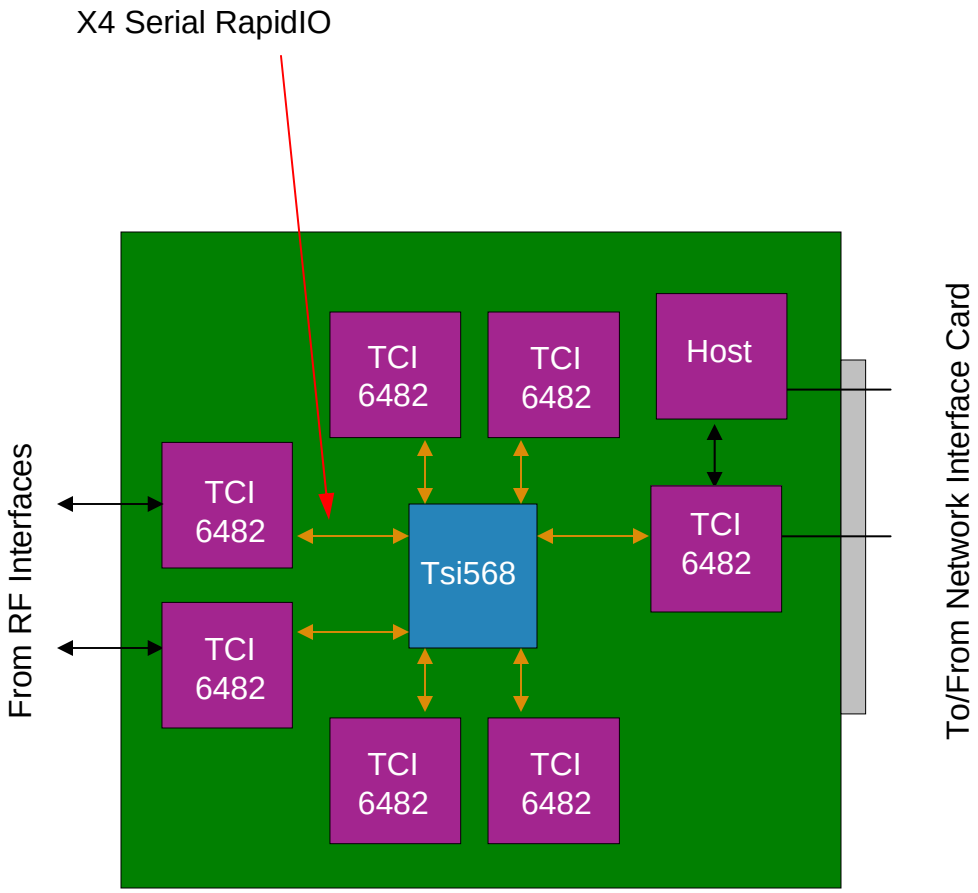
Baseband Interconnect

- Serial RapidIO presents the following advantages
  - 3 layer protocol terminated in hardware allows all the DSP processing power to be focused on symbol and chip rate processing
  - Switch fabric Look-Up-Table can be updated for dynamic load balancing amongst DSPs (critical as traffic can dynamically can change e.g. between voice vs data)
  - 4-level prioritization allows for high priority traffic (e.g. call signaling or voice traffic) to supercede low priority traffic (e.g. data traffic)
  - Streaming writes in RapidIO (using data-only Type 6 packets) allow low-overhead data transfer

DSP Switching

Baseband Processing

- Much higher complexity requirements (e.g. Multi-User Detection) and more dynamic environment: **Serial RapidIO allows dynamic load balancing**
- Blurred lines between Chip Rate and Symbol Rate: **built for Peer-to-Peer communication**
- Higher channel density (e.g. 96 AMR channels): **High throughput x4 serial RapidIO links**



Algorithm Load Balancing

- CDMA IS-95 supported single-user algorithms and ignored Multiple Access Interference (MAI)
- WCDMA at higher data rates requires sophisticated multi-user algorithms for channel estimation and detection
- Multi-user algorithms involve complex matrix multiplications and inversions

Algorithm Load Balancing

- More channel density and greater computing complexity
- Baseband processing is now about distributed processing
- Some algorithms (e.g. for multi-user estimation and detection) may have to be loaded balanced across >1 DSP
- Let’s break down large algorithmic blocks

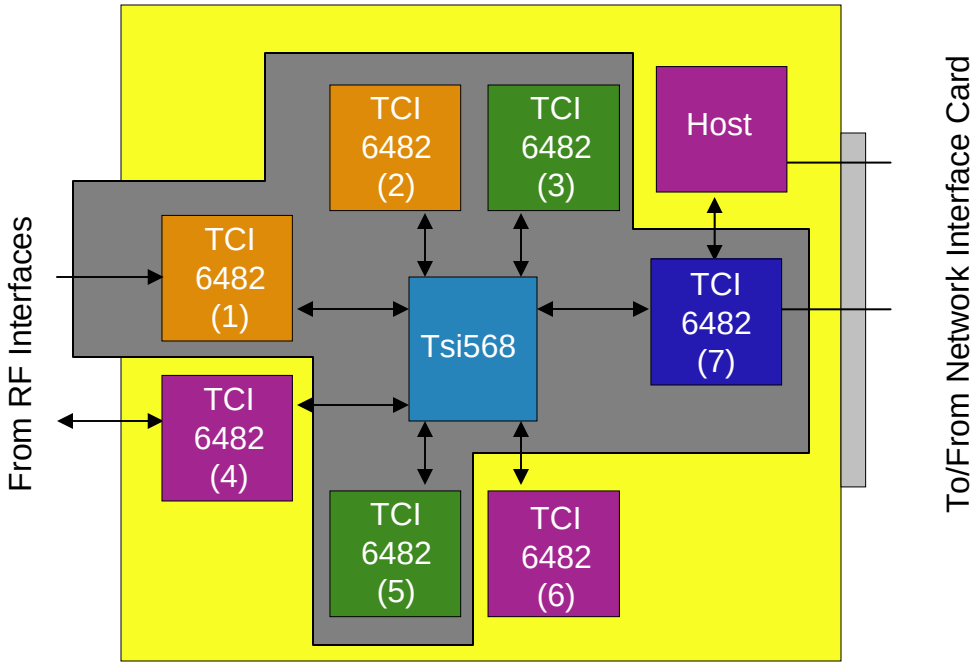
Algorithmic Blocks

- Correlation (Frequency Synchronization)
- Multipath Estimation (Auto-correlation, known pilot references to find multi-paths)
- Multi-User Detection (Using short scrambling codes and channel estimates, iterative)
- Pilot Symbol Extraction
- Channel Estimation (Cross-correlation, performed at each Rake finger output)
- QPSK de-modulation and Maximal Ratio Combining
- De-interleaving
- Viterbi or Turbo Decoding

Receive Processing Loading

Baseband Processing - Rx

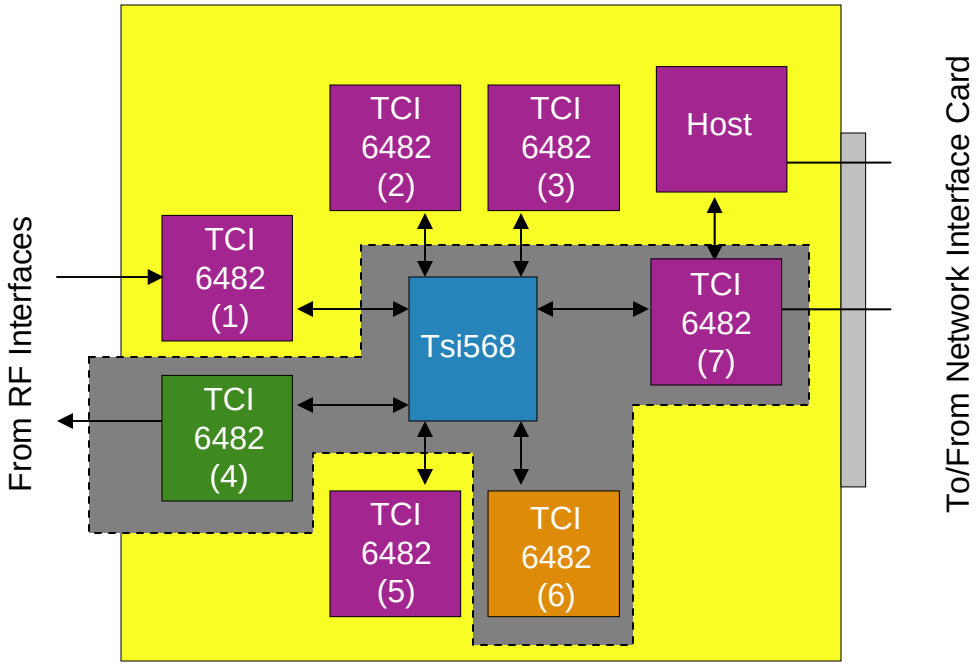
- Correlation and Multipath Estimation in DSP-1 and DSP-2 (Rake receivers and de-spreading)
- Pilot Symbol Extraction, Channel Estimation and Multi-user detection handled in DSP-3 and DSP-5 with frequent updates between them
- QPSK de-modulation and MRC in DSP-5
- Symbol rate processing (Turbo and Viterbi decoding) in DSP-7
- Closed loop power control communication from DSP-1 to DSP-4



Transmit Processing Loading

Baseband Processing - Rx

- **Coding and FEC on DSP-6**
- **QPSK modulation and spreading on DSP-4**
- **Closed loop power control communication from DSP-1 to DSP-4**



Conclusions

- Transmit and Receive can be flexibly implemented on a single card
- Chip rate and symbol rate processes can be allocated to specific processors (more efficient) or re-assigned dynamically (more flexible, more context switching)
- Algorithms and data paths can be updated through software upgrades
- Initial card software de-bug is more easily managed (data paths and algorithms can be tweaked)

Conclusions

- **Pressures on inter-processor communication performance**
  - **More Interference Cancellation = More users (more traffic and higher capacity requirements)**
  - **Increases in Channel density (higher capacity requirements)**
  - **New higher bandwidth data protocols (e.g. HSUPA)**
  - **More users = more interference cancellation (higher processing complexity)**