

SEE  
THE **FUTURE.**  
CREATE YOUR OWN.

# Serial RapidIO for DSP to DSP Communication

Travis Scheckel  
Wireless Infrastructure  
Texas Instruments  
[t-scheckel@ti.com](mailto:t-scheckel@ti.com)



# Agenda

- ◆ **Overview of Serial RapidIO**
- ◆ **Serial RapidIO Capabilities on TMS320TCI6482**
- ◆ **System Design Considerations and Ensuring Success**
- ◆ **Documentation and Deliverables**

# Overview of Serial RapidIO

# RapidIO History

- ◆ **RapidIO Trade Association was formed in 2000**
- ◆ **Mission: Develop a reliable, high-performance, packet-switched, interconnect technology for the embedded industry.**
- ◆ **Initial specification released in early 2001, serial spec released in early 2002.**
- ◆ **TI Joined the Technical Working Group in late 2001, Steering committee in 2003**
- ◆ **TI will sample the 1<sup>st</sup> RapidIO enabled DSP in 2Q05**

# Requirements of an Embedded System Interconnect

## ◆ Performance

- High-Bandwidth Point-to-point
  - Parallel busses limited
- Low protocol overhead
- Lowers software complexity

## ◆ Broad adoption

- Non-proprietary, multi-vendor support
- Established Embedded Interconnect
- Re-use across multiple chips, boards, systems & platforms

## ◆ Robustness and Reliability

- System-level Error management
- Loss-less Protocol

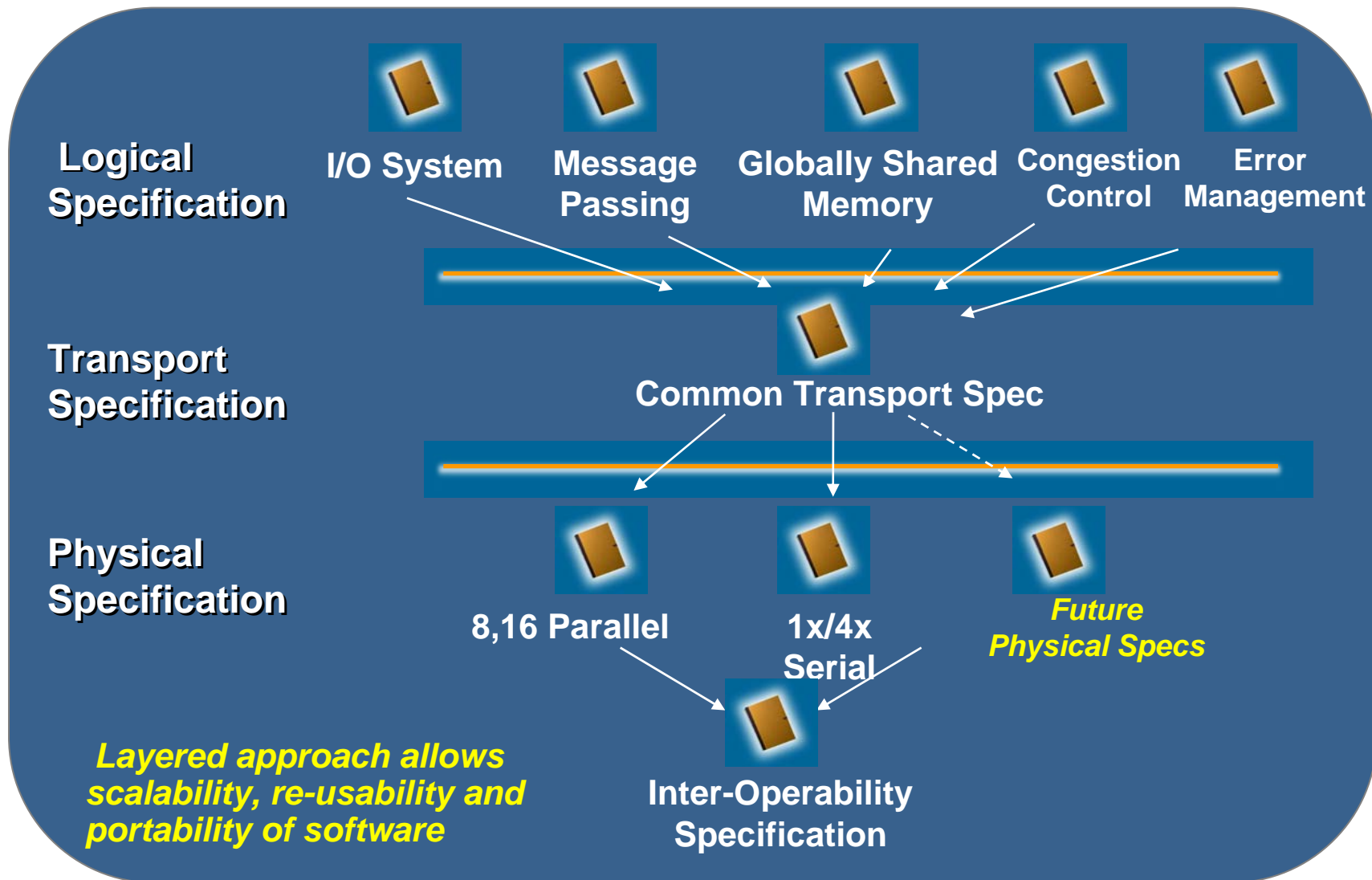
## ◆ Flexibility

- Scalable bandwidth
- Distributed Processing with multiple OS's
- Multiple Topology support
  - Peer-to-peer support
  - Backplane support
- Packet type functionality

## ◆ Reduced system cost

- Merged control & data backplane
- Low chip cost
  - Small silicon footprint
  - Few pins
  - Low power/bandwidth

# RapidIO Specification Hierarchy – Layered Approach

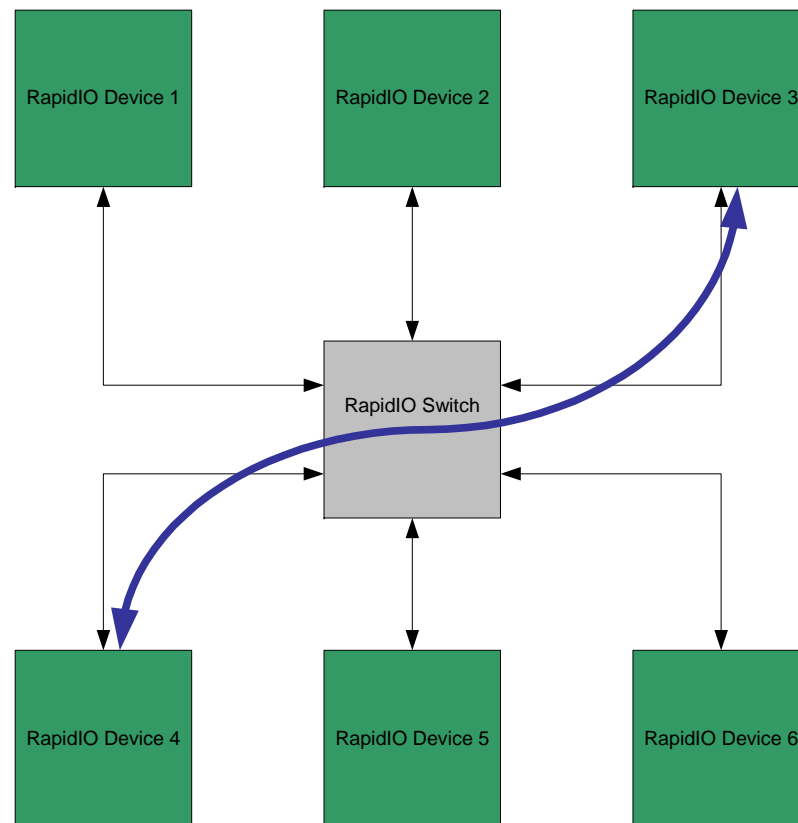


# Serial RapidIO Physical Layer

- ◆ **Rev 1.2 Serial Spec**
- ◆ **Based on IEEE 802.3ae XAUI Electrical Specs**
- ◆ **1.25, 2.5, or 3.125Gbps data rates**
- ◆ **1X and 4X port widths**
- ◆ **AC coupled interface, 500mV – 2000mV peak-to-peak differential swing**
- ◆ **8b/10b Encoded Data with Clock Recovery**
- ◆ **CRC Protection and Hardware Error Recovery**
- ◆ **Short Run and Long Run specifications**

# RapidIO Transport Layer

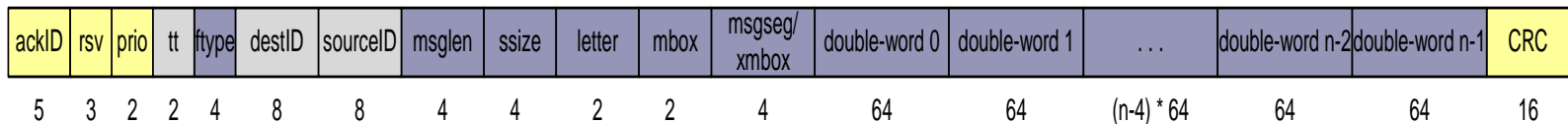
- ◆ **Common Transport**
  - 8 or 16 bit device IDs
  - Destination routing not influenced by topology



# RapidIO Packet Formats

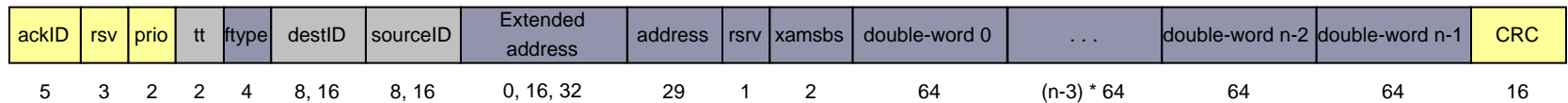
## ◆ Logical Packet Types

- Scalable packets to 256 Byte payloads
- DMA (Direct IO) protocol
  - NWRITE, NWRITE\_R, SWRITE, NREAD, ATOMIC
- Messaging protocol – up to 16 packets per message
- Maintenance operation



*For Message Passing*

Type 11 Message Class

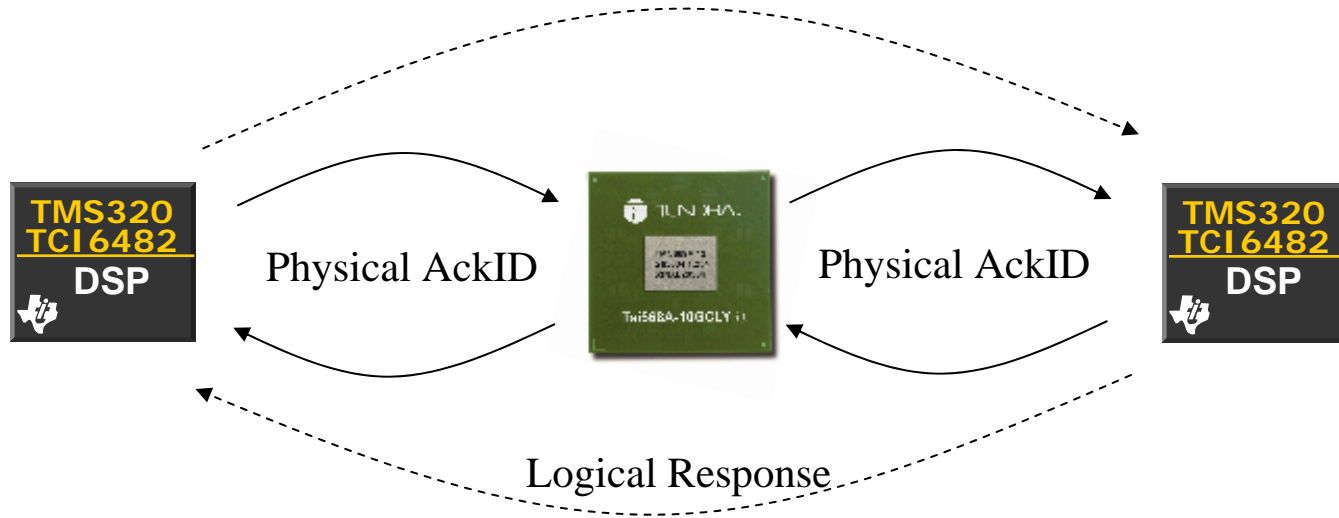


*For Direct IO*

Type 6 - Streaming-Write Class

Physical layer
  Transport layer
  Logical layer

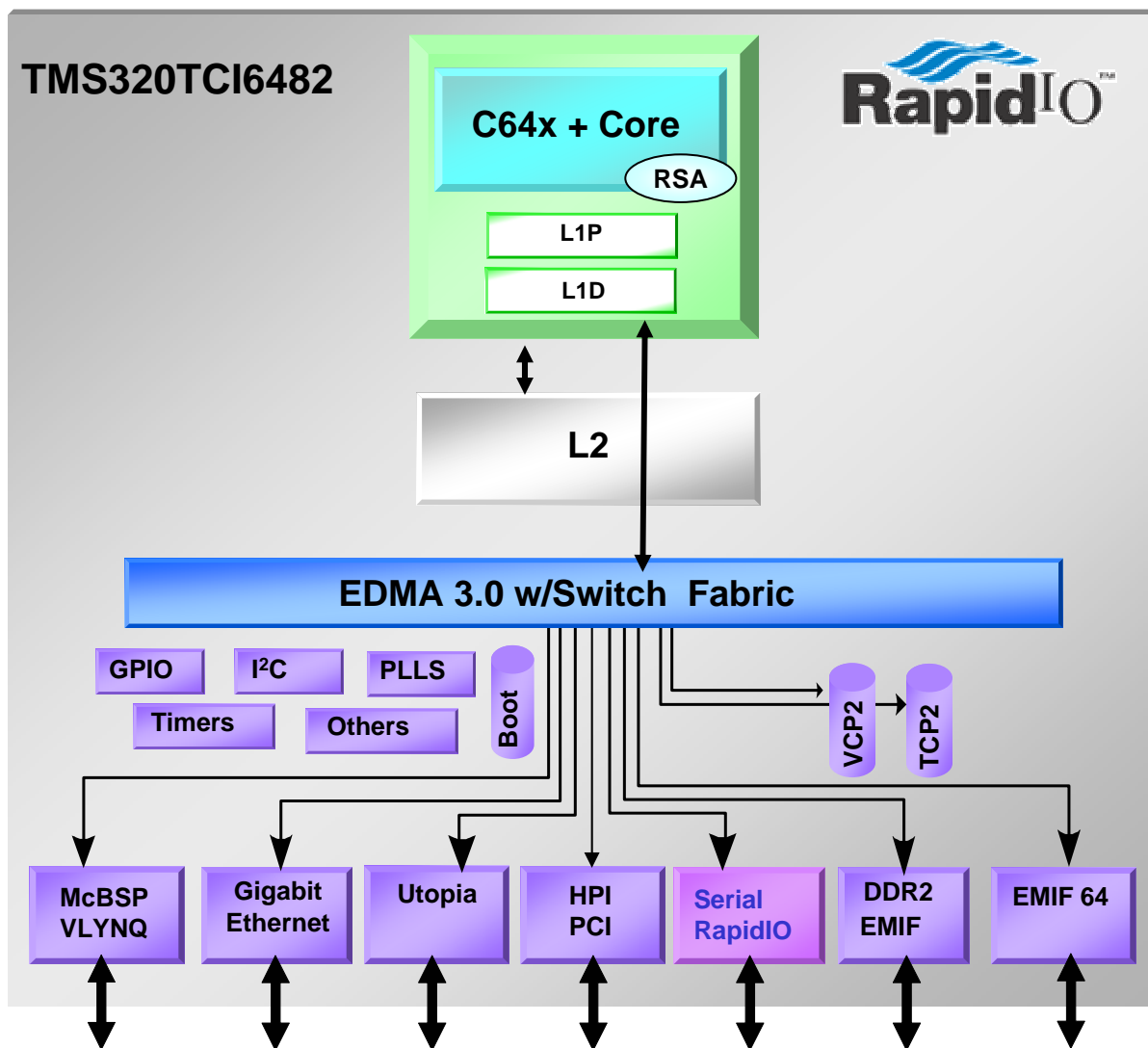
# Physical and Logical Layer Acknowledges Offer Reliability



- ◆ **Physical AckID is 5-bit sequential numbering between link partners**
  - Used for Retry mechanism (CRC error, Full buffer)
  - CRC does not cover AckID field, no re-generation needed
- ◆ **Logical layer responses between source and destination**
  - NREAD, NWRITE\_R, Messages
  - Used for receipt notification versus higher layer software stack

# Serial RapidIO Capabilities on TMS320TCI6482 DSP

# DSP Block Diagram: TMS320TCI6482 DSP



- ◆ **C64x+ DSP Core @ 1 GHz**
- ◆ **Power ( 3.0w target )**
- ◆ **Memory**
  - 32 KB L1 Prog. memory
  - 32 KB L1 Data memory
  - 2 MB L2 Local memory
  - 16 KB Boot ROM
- ◆ **Communications Subsystem**
  - 1x/4x SRIO
  - Gigabit Ethernet RGMII
  - UTOPIA II
  - DDR2-533 (32-bit EMIF)
  - 64-bit EMIF (SDR)
  - HPI, PCI-66MHz
  - I2C
- ◆ **On Chip I P blocks**
  - EDMA w/ Switch Matrix
  - VCP2, TCP2, RSA

# TMS320TCI6482 DSP RapidIO Features

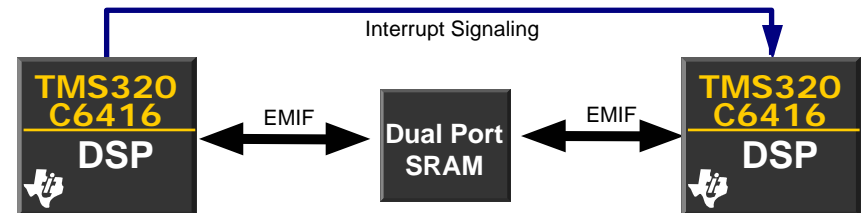
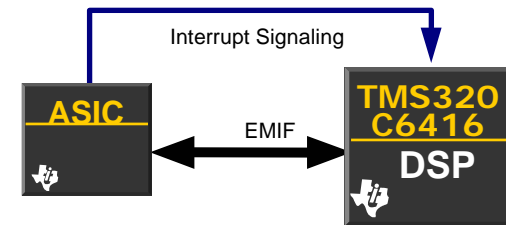
- ◆ **RapidIO Specification v1.2 Compliant, Errata 1.2**
- ◆ **(4) 1X ports configurable to a 4X Serial RapidIO port**
- ◆ **Support for 1.25, 2.5, and 3.125Gbps rates**
- ◆ **Support for 8b and 16b device ID**
- ◆ **Support of 34, 50, and 66b addresses**
- ◆ **Packet payloads up to 256B**
- ◆ **Direct IO transfers**
  - **Supporting 4 simultaneous non-posted transactions**
  - **Hardware segmentation function for 4KB transfers**
- ◆ **Message passing transfers**
  - **Multi-segment messages up to 16 packets**
  - **Single-segment message support for 64 mailboxes/4 letters**
  - **Security features for restricting RX queues based on SourceID**
  - **16 Rx/Tx Queues (weighted round robin)**

# Features continued..

- ◆ **Support for Multi-cast with a second supported DeviceID**
- ◆ **Powerdown support for un-used Serdes, ports, or functional blocks**
- ◆ **DOORBELL interrupts**
  - **User defined ISCR bit (64 assignable bits)**
- ◆ **Time-based interrupt pacing mechanism**
  - **Programmable down counter**
- ◆ **Error Management Extensions**
- ◆ **Congestion Control Extensions**
- ◆ **JTAG access to SerDes Test Features**
  - **Built-in SerDes test/debug features including Loopback, PRBS, internal power supply monitor and Eye Scan**
- ◆ **1149.6 AC coupled JTAG support**

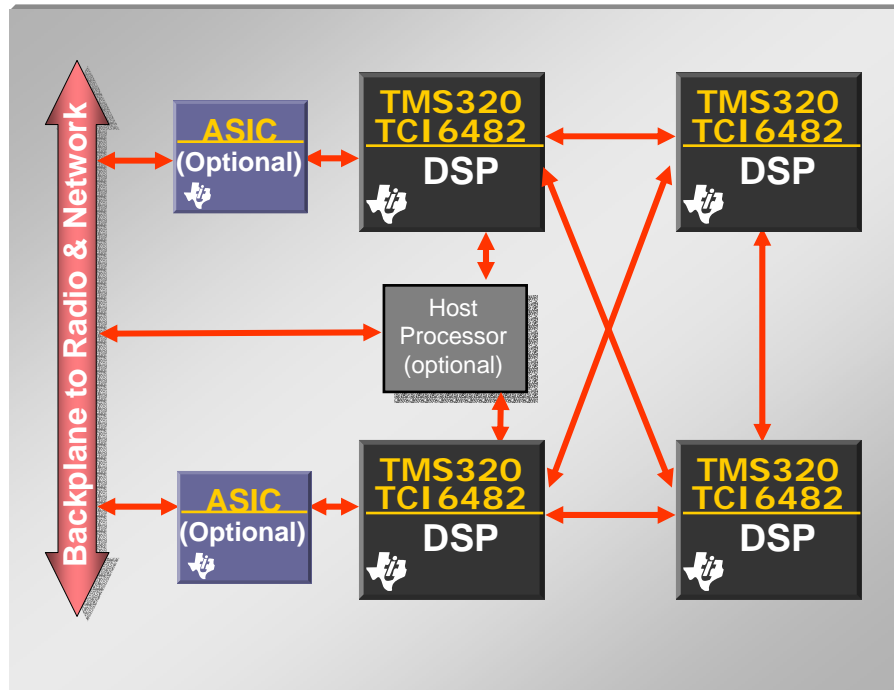
# Past DSP Interfaces

- ◆ High bandwidth limited to EMIF, or PCI
  - Half duplex
  - Push versus Pull
- ◆ Non-optimized for chip-to-chip
  - Out of band Interrupt
- ◆ Limited number of devices
  - Load limited
  - No multi-cast support



# RapidIO System Level Usage

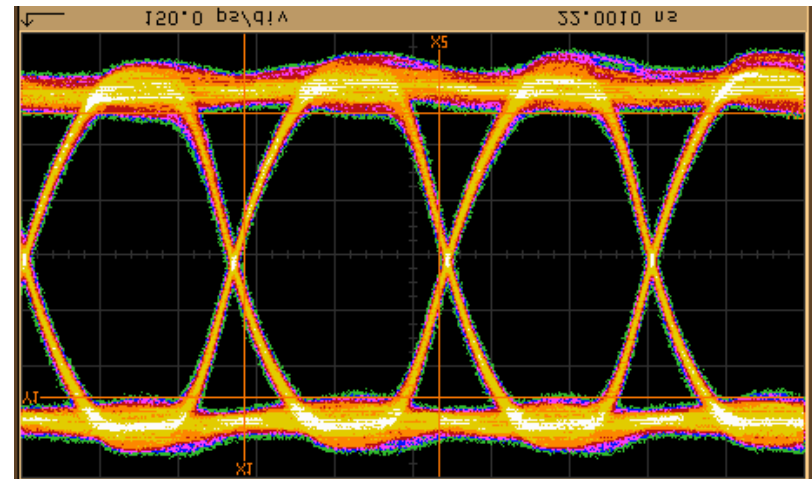
- ◆ **Dataflow (Push or pull)**
- ◆ **Memory Management**
  - **Direct I/O Logical Specification**
    - Target memory address is specified
    - Memory map knowledge required
  - **Message Passing Logical Specification**
    - Only mailbox numbers are specified
    - Destination Device is responsible for storing and managing memory space
- ◆ **Interrupt Handling**
  - In-band Interrupt Notification (Doorbell)
  - Automatic Interrupt Generation for Message Passing
    - Configurable rate
- ◆ **DSP/BIOS™ Support**
  - MSGQ (Message Queue) – new module for local and remote message passing
  - Transparent of the Transport



# System Design Considerations and Ensuring Success

# TI's Serdes Technology Proven Design Practices for Success

- ◆ **Serial RapidIO Takes Advantage of TI's Strong Industry Leading SerDes Technology**
  - **Self-contained SERDES block**
    - Allows crosstalk isolation from other signals
    - Dedicated bumps for analog power supplies
  - **Reference Clock Distribution(RCD) macros**
    - Uniquely created per design to distribute clock to SERDES
    - Add significant decoupling of core supply to minimize jitter
  - **Reducing on-chip noise**
    - Core decoupling caps and DECAP filler cells for reducing power supply noise
    - I/O placement rules for reducing substrate noise
  - **Flip-chip optimized**
    - Controlled impedances and good signal integrity
    - Better power isolation and distribution with less IR drop



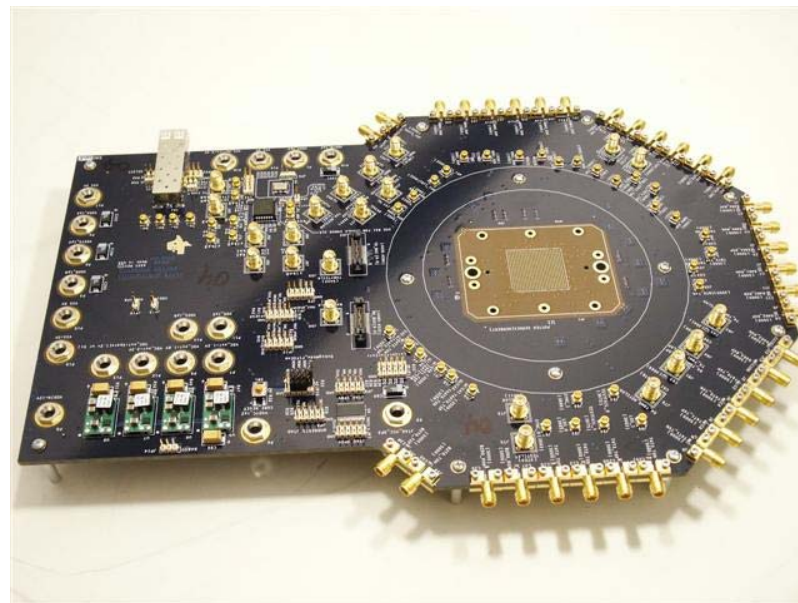
# Verification/Validation

- ◆ **Module Verification**
  - Functional coverage and protocol compliance
  - RapidIO Trade Association BFM and compliance checklist
- ◆ **Chip Verification**
  - Chip level functionality and performance
  - QuickTurn emulation of CPU, DMA and RapidIO peripheral
  - Software validation
- ◆ **System and Interoperability Testing**
  - Internal verification and debug board
  - External ATCA Interoperability and prototype platform with Ensemble2™



# High-speed Design Requirements

- ◆ **With all the positives of SerDes, there are some important design considerations**
  - **There are three main areas to address:**
    - **High-quality Reference Clock needed**
      - Low jitter requirements
      - Careful on-board and on-chip distribution
    - **High-speed Signal Routing Board Requirements**
      - Differential Signaling 1.25 – 3.125Gbps
      - Board Stack-up, Signal Integrity and Controlled Impedance Important
      - Cross talk considerations
    - **Power filtering**
      - On-board and on-package decoupling
  
- ◆ **Test and debug capabilities**
  - **Serial test and debug lab equipment will be needed**



# Documentation and Deliverables

# RapidIO Collateral

- ◆ **RapidIO Module Peripheral Guide**
  - Detailed functional description
- ◆ **High-speed Board Design Guidelines**
  - Board layout and stackup requirements
- ◆ **TI DSP Starter Kit**
  - Reference Design board with two TMS320TCI6482 DSP Devices
- ◆ **DSP/BIOS™ User's Guide**
  - MSGQ Documentation

- ◆ **RapidIO offers tremendous benefits as an embedded system interconnect**
  - Rich feature set
  - Control and data path connectivity
- ◆ **Ecosystem is real**
  - Introduction of the TMS320TCI6482 DSP
  - RapidIO device portfolio includes switch, bridge, processor and FPGA silicon
  - Software and test support
- ◆ **Further Info**
  - RapidIO Building a Successful Ecosystem for Embedded Applications Panel Discussion, 2:00pm
  - “Birds of a feather” roundtable session 7:00pm

Travis Scheckel  
WI Systems  
Texas Instruments  
t-scheckel@ti.com

Get to market faster  
with TI products,  
support and partners.



SEE THE **FUTURE.**  
CREATE YOUR OWN.