

RapidIO™ Solutions for Wireless Infrastructure

CHALLENGE: Provide a standard, high-bandwidth, low-latency interconnect solution for next-generation wireless infrastructure development

Regardless of which wireless standards become dominant in next-generation wireless networks, two facts are clear: high-speed data will become a more dominant traffic type and the demand for voice channels will continue to increase. Provisioning for this increased mix of voice and data traffic is driving dramatic increases in compute density requirements in wireless infrastructure. The transition from predominantly voice traffic to a mix of voice and high-speed data, coupled with the need for increased capacity, will result in a substantial increase in the amount of signaling among nodes in the network. The monolithic, bus-based compute architectures of the past that connected processing elements together in systems will not survive the transition.

Coincident with this transition is an economic trend toward lower cost per channel that is driving new standards development and encouraging equipment manufacturers to cede control of proprietary subsystems to standard, off-the-shelf solutions. Equipment manufacturers require a new industry standard interconnect technology that offers high bandwidth, low processing and protocol overhead, and low implementation cost to constrain the potential impact of deploying off-the-shelf systems and to enable new time-to-market advantages previously unattainable with proprietary technologies.

SOLUTION: RapidIO Interconnect Speeds System Throughput

The RapidIO interconnect was developed jointly by leading semiconductor and system vendors to meet the connectivity requirements for next-generation communication systems. The RapidIO interconnect is ideally suited for wireless infrastructure applications due to these features:

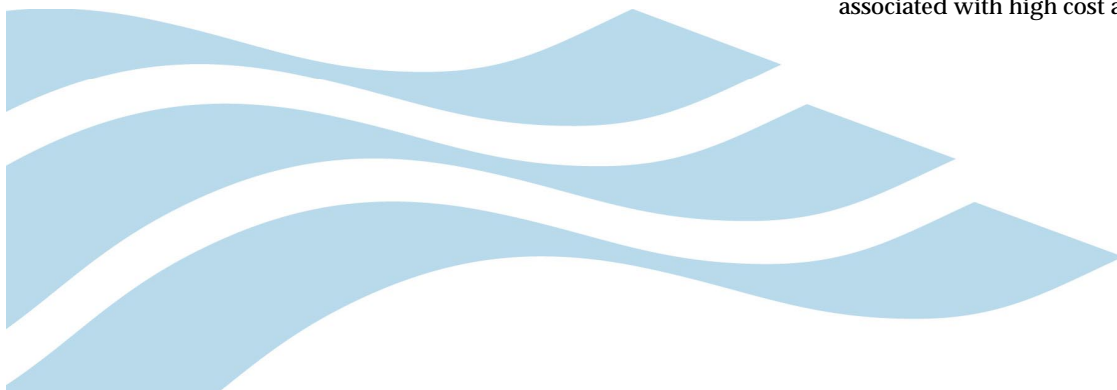
- Scalable bandwidth of 1 to 60 Gigabits per second
- Low protocol overhead
- Reliable transport that reduces system software burden
- Low latency connections between devices and through switches
- Optimized for chip-to-chip and board-to-board connections (across backplanes)
- Direct integration on leading microprocessor, DSP and FPGA products
- True peer-based system architecture model

Specifically, the RapidIO interconnect can provide the following connectivity in wireless infrastructure applications:

- DSP farm connectivity
- Peer-to-peer or master/slave connectivity between processors, communications processors, network processors, ASICs and FPGAs
- Control and data backplane connectivity
- Baseband to RF board interconnect
- Chip to symbol rate processor interconnect

EXAMPLE: RapidIO in a 3G Wireless System

Figure 1 provides a conceptual view of a 3G base station architecture illustrating the connection of baseband processing elements. Here, a combination of ASICs, FPGAs, and/or DSPs provide the resources for chip-rate and symbol-rate processing and are typically connected via proprietary bus interfaces. This configuration is associated with high cost and a low degree of flexibility.



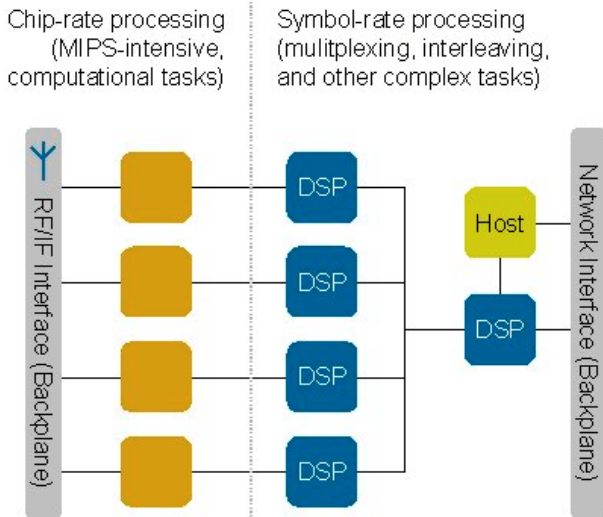


Figure 1: Current 3G simplified architecture

In contrast, Figure 2 provides a conceptual view of the same 3G architecture employing RapidIO. Here, the interfaces between the Radio Element (the antennas in the diagram), the chip rate processors, the chip rate DSPs, and the symbol rate DSP(s) employ RapidIO as their interconnect. Off-the-shelf components or subsystems can communicate seamlessly. This architecture provides both scalability, lower cost, and much faster time-to-market while still meeting the bandwidth and latency demands of the application.

The use of the RapidIO interconnect in a baseband board design creates a homogeneous interconnect environment, providing even more connectivity and control among the components. RapidIO is based on the memory and device addressing concepts of processor buses where the transaction processing is managed completely by hardware. This enables the RapidIO interconnect to provide the lower latency, reduced overhead of packet data processing, in combination with high system bandwidth. All of these attributes are key for wireless infrastructure processing tasks, especially with voice and video convergence.

In addition, unlike traditional bus interfaces, the RapidIO interconnect offers very low pin count interfaces with scalable system bandwidth based on 10 Gigabit per second bi-directional links.

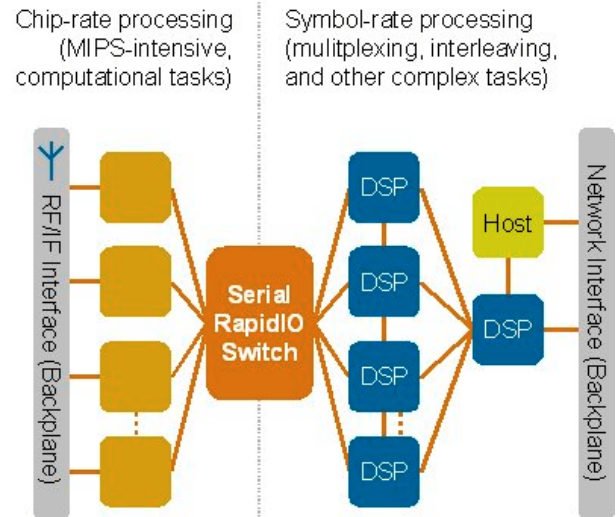


Figure 2: RapidIO-enabled 3G architecture

RESULTS: The Benefits of RapidIO Deployment

- **Get to market quicker:** RapidIO-enabled products, a variety of which are available now, simplify system design and reduce integration issues.
- **Increase system performance:** Targeted for embedded application performance requirements, RapidIO enables low latency, high-bandwidth solutions.
- **Reduce risk:** The broadly supported RapidIO standard has been adopted by ECMA as ECMA-342 standard for system interconnect and the RapidIO 1.2 Specification has been approved by the International Standards Organization as ISO/IEC18372.
- **Reduce R&D costs:** The RapidIO interconnect eliminates the need for high-priced fabrics or proprietary backplane interconnects by enabling off-the-shelf, interoperable, cost-efficient solutions.

About RapidIO Technology

The RapidIO interconnect architecture, designed to be compatible with the most popular integrated communications processors, host processors, digital signal processors, and bridge chips, is a high-performance, packet-switched, interconnect technology. It addresses the embedded industry's need for high performance, low overhead, reliable serial interconnect technology.

Interested companies are invited to join the RapidIO Trade Association, a non-profit corporation controlled by its members. Go to: WWW.RAPIDIO.ORG