

RapidIO™ Solutions for Disk Storage Systems

CHALLENGE: Unclogging the data transfer bottleneck in RAID arrays and other mass storage systems with ultra-high availability and data integrity

High data throughput and data integrity have traditionally made the connections between mass storage system components a design challenge. Over the past few years, storage-hungry applications have spurred a rapid escalation of system-level performance goals.

Parallel architectures have traditionally been used to implement these systems. But as bus speeds increase and on-chip physical I/O components such as SerDes (serializer/deserializer) demonstrate their ability to move data on and off chips at hundreds of megabits per second, parallel buses designed for personal computer applications have hit the performance wall.

The inability of the present generation of parallel bus architectures to operate reliably above 133 MHz has limited the data transfer rates for disk arrays and other high-performance mass storage devices. The traditional solution for parallel architectures – increasing bus width – presents design engineers not just with significant signal-integrity and inter-bus skew problems but also with the complex task of managing signals on a wide bus. Figure 1 illustrates a common storage architecture with a 64-bit PCI or proprietary parallel bus and protocol.

Performance and data integrity are critical. But performance is more than sustained data throughput. Also included are metrics such as latency, burst rate, flexibility, scalability, and reliability. Next-generation bus architectures will succeed only if they: (1) are open-standards based; (2) enable quick design cycles; (3) preserve application-layer legacy software; (4) keep development costs low; and (5) offer a scalable solution.

SOLUTION: Serial RapidIO interconnect speeds system throughput

Developed jointly by leading semiconductor and system vendors to handle the connectivity and

reliability challenges of mass storage systems, the serial RapidIO interconnect offers the following features that make it well suited for storage as well as many other applications.

- Software independent – looks like a bus to software
- Scalable to 64,000 devices
- Scalable bandwidth of 1 to 60 Gigabits per second
- Low latency connections between devices and through switches
- Optimized for chip to chip and board to board connections (across backplanes)
- Hot-swap capability
- Robust error detection and recovery
- Ultra-high reliability

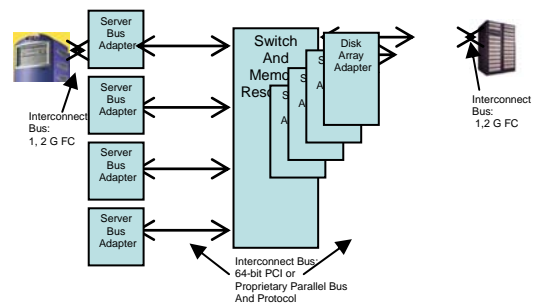


Figure 1: Current storage architecture

APPLICATIONS: RapidIO Interconnect Applications in Mass Storage Systems

The serial RapidIO Interconnect is suitable for the following applications in mass storage systems such as RAID arrays.

- 24/7 database applications
- A/V on-demand repositories for medical imaging systems
- High-definition video editing, streaming, and processing
- Web, e-mail, and news servers
- Financial applications

- Clustering environments
- Workgroup/File Server

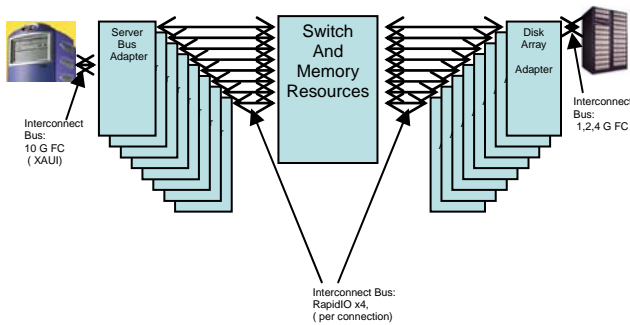


Figure 2: RapidIO storage application solution

As shown in Fig.2, by using serial RapidIO connections, multiple lane links connect server bus modules to the system's switch fabric infrastructure. Similarly, the serial RapidIO fabric connects to the disk-array adapters. A four-lane RapidIO link running at 3.125 Gigabits per second can deliver 10 Gigabits per second system throughput with full data integrity.

Because serial RapidIO is similar to microprocessor buses – memory and device addressing instead of the software management of LAN protocols – packet processing is implemented in hardware. This means significantly lower I/O processing overhead, lower latency and increased system bandwidth. But unlike most bus interfaces, RapidIO has low pin count interfaces and scalable bandwidth based on 3.125 gigabit per second bi-directional links.

Using serial RapidIO reduces packet-data latency and overhead. As a result, it is the interconnect of choice for high-performance storage applications where latency is a primary cause of bottlenecks.

RESULTS: Benefits of Serial RapidIO Deployment in Mass Storage Systems

Get to market quicker

- Significant product support from semiconductor manufacturers.
- Components and systems available now.
- Standard is stable and internationally certified.
- Interoperability is assured in open standard.

Increased system performance

- Innovative contributions from a number of member companies with extensive experience in embedded switched fabrics raise the level of functionality and performance.
- RapidIO targets embedded application performance requirements resulting in a low

latency, small footprint, and low-power interconnect.

- Boosts efficiency of communications networks:
 - Reduces total number of processors
 - Harnesses full capacity of processors
 - Simplifies system architecture and management

Reduced Risk

- Widely adopted global standards are crucial to customers developing next-generation wireless systems.
- The RapidIO standard has been adopted by ECMA as ECMA-342 standard for system interconnect; ISO approval in process.
- Broad range of support from: general purpose processors, network processors, DSPs, and FPGAs will assure interoperability.
- OEM participation in standards development process helps ensure that the RapidIO interconnect will meet critical embedded requirements for cost, performance, and reliability.

Reduce internal R&D costs

- RapidIO provides a high-performance, commercial off-the-shelf solution to reduce OEM development costs and time-to-market.
- RapidIO targets price/performance needs of real-time embedded applications.
- The performance of RapidIO eliminates dependence on high-priced internally developed proprietary switch fabric solutions.
- Heterogeneous processing support (RISC, DSP, NP, and FPGA) eliminates the need for multiple dissimilar interconnects.

About RapidIO Technology

The RapidIO interconnect architecture, designed to be compatible with the most popular integrated communications processors, host processors, networking digital signal processors, and bridge chips, is a high-performance, packet-switched, interconnect technology. It addresses the high-performance embedded industry's need for high performance, low overhead, reliable serial interconnect technology. The RapidIO interconnect allows chip-to-chip and board-to-board communications at performance levels scaling to 10 Gigabits per second and beyond.

Interested companies are invited to join the RapidIO Trade Association, a non-profit corporation controlled by its members.



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