Freescale T-Series and B-Series Products with RapidIO
28nm Products: T4240 and B4860 (9164)

**Description**
Multicore networking processor for control, datapath and application layer processing in routers, switches, gateways and embedded computing

**Cores and IP**

<table>
<thead>
<tr>
<th>Description</th>
<th>T4240</th>
<th>B4860</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cores and IP</td>
<td>12 e6500 64-bit dual-threaded 1.8GHz cores + AltiVec w/ 6 MB total L2</td>
<td>4 e6500 1.8GHz cores w/ 2 MB shared L2</td>
</tr>
<tr>
<td></td>
<td>Datapath acceleration architecture (DPAA) w/ Fman, Qman, Bman and Rman, PME, DCE, security 1.5MB L3, 800 MHz platform</td>
<td>6 SC3900 1.2GHz DSP cores w/ 6MB shared L2</td>
</tr>
<tr>
<td></td>
<td>3 DDR3 64b 2.133 GHz controllers w/ ECC</td>
<td>DPAA + MAPLE B3 baseband accelerator</td>
</tr>
<tr>
<td></td>
<td>32-lane 10Gb/s SERDES, dual USB2.0 PHY</td>
<td>1MB L3, 667 MHz platform</td>
</tr>
</tbody>
</table>

**Power**

- <60W power at 1.8 GHz
- <30W power in standard mode

**Package**

- 1932 pins, 45x45x3.18mm body size, 1mm C5 pitch
- 1020 pins, 33x33x2.78mm body size, 1mm C5 pitch
**Industry Leading Cores Performance**

**e6500 High-Performance MPU**
- 64-bit Power Architecture® core
- Dual threads provide x1.7 times the performance of a single thread
  - Clustered L2 cache allowing strict allocation or full sharing
- AltiVec 128b SIMD unit

**SC3900 High-Performance DSP**
- Step function in DSP performance over previous generation and competition
- State-of-the-art support for control code with Branch Prediction
- MMU and address translation support
- Clustered L2 cache allowing strict allocation or full sharing

**High Speed Accesses to Memories**

**Low Power Design**

BDTI recently benchmarked the SC3900 core included in the Freescale B4860. Running at 1.2 GHz, the SC3900 core received a BDTIsimMark2000™ score of 37,460 – the highest speed score recorded. See [www.BDTI.com](http://www.BDTI.com) for details.
QorIQ Qonverge B4860 – Block Diagram & Benefits

- Next generation, e6500 Dual-Thread Power Architecture® cores offer highest CoreMark/Watt with AltiVec technology for dramatic L2 scheduling acceleration
  - Next generation, SC3900 StarCore provides 2x DSP performance compared to competitive offerings
  - Above 21 GHz of programmable performance
  - Smart hardware acceleration for Layer 1, 2, Control and Transport allows for best in class performance, power and cost
- Large scale SoC integration allows for simpler programming models and easier load balancing
- Integrated, rich I/O including backhaul & antenna interfaces provides flexibility, interoperability and reduces overall system cost
## The High-End—Driving the Cloud...

### Control Plane Focus

- Control & Data Plane
- **e600 +Soc**

### Network Services

- **New** QorIQ – P5
  - P5040 / P5021
- QorIQ – P5
  - P5020 / P5010
- **New** QorIQ – P4
  - P4080
  - P4040
- **T4 Family**
  - T4240
  - T4160

### Maximum Transactions Core-to-memory & Packet processing

### Increasing Performance

### Service Provider

- Core/ Edge Routing
- Aggregation
- Transport

### Datacenter

- WAN Optimization
- ADC/SLB
- Monitoring

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QorIQ T4240
– A Look Under the Hood

CoreNet Coherency Fabric

<table>
<thead>
<tr>
<th>Security Fuse Processor</th>
<th>Security Monitor</th>
<th>2x USB 2.0 wPHY</th>
</tr>
</thead>
<tbody>
<tr>
<td>IFC</td>
<td>Power Management</td>
<td>SD/MMC</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2x DUART</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2x I²C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SPI, GPIO</td>
</tr>
<tr>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>512KB CoreNet Platform Cache</th>
<th>64-bit DDR3 Memory Controller</th>
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<th>64-bit DDR3 Memory Controller</th>
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</table>

Peripheral Access Mgmt Unit

<table>
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<th>512KB CoreNet Platform Cache</th>
<th>64-bit DDR3 Memory Controller</th>
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</table>

Pre-fetch

<table>
<thead>
<tr>
<th>512KB CoreNet Platform Cache</th>
<th>64-bit DDR3 Memory Controller</th>
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</table>

16-Lane 10 GHz SerDes

16-Lane 10 GHz SerDes
## Enhancing Core Performance with Data Path Acceleration Architecture

### Hardware Accelerators

<table>
<thead>
<tr>
<th>Accelerator</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>FMAN</strong></td>
<td>Frame Manager: 50 Gbps aggregate Parse, Classify, Distribute</td>
</tr>
<tr>
<td><strong>BMAN</strong></td>
<td>Buffer Manager: 64 buffer pools</td>
</tr>
<tr>
<td><strong>QMAN</strong></td>
<td>Queue Manager: Up to $2^{24}$ queues</td>
</tr>
<tr>
<td><strong>RMAN</strong></td>
<td>Rapid IO Manager: Seamless mapping sRIO to DPAA</td>
</tr>
<tr>
<td><strong>SEC</strong></td>
<td>Security: 40Gbps: IPSec, SSL Public Key 25K/s 1024b RSA</td>
</tr>
<tr>
<td><strong>PME</strong></td>
<td>Pattern Matching: 10Gbps aggregate</td>
</tr>
<tr>
<td><strong>DCE</strong></td>
<td>Data Compression: 20Gbps aggregate</td>
</tr>
<tr>
<td><strong>Saving CPU Cycles</strong></td>
<td>For higher value work</td>
</tr>
</tbody>
</table>

**New**

**Enhanced**
T-Series Target Markets, Key Features

Balanced Architecture
- High-performance dual threaded 64b cores
- Multicores up to 1.8GHz with 128b AltiVec
- Power Efficiency
- 4x performance of P4080 App Accelerators
- CoreNet On-chip Fabric
- Designed to efficiently “feed” the cores
- Eliminates bus contention

High Speed Interconnect
- RapidIO, PCIe, XAUI, XFI, Interlaken, SATA

Tightly Coupled Cache Hierarchy
- Optimum banked and tiered memory architecture
- Cores are closer to the data to reduce latency

High-Performance Virtualization
- Advanced Core and SoC
- Software solutions designed for AMP

The T4240 and T4160 Processors are architected to provide Best in Class performance within an embedded power envelope
### QorIQ – T4240
Market Leading Compute Density

#### x86 Thermal Performance Throttling

#### QorIQ Thermal Independent Performance

#### Compute Density per Blade at Equivalent Power

<table>
<thead>
<tr>
<th>Processor</th>
<th>Tjunc</th>
<th>25</th>
<th>30</th>
<th>35</th>
<th>40</th>
<th>45</th>
<th>50</th>
<th>55</th>
<th>60</th>
<th>65</th>
<th>70</th>
<th>75</th>
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<tbody>
<tr>
<td><strong>Intel i7 2600</strong></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMark</td>
<td>61,000</td>
<td>58,000</td>
<td>58,500</td>
<td>57,000</td>
<td>55,500</td>
<td>52,000</td>
<td>48,000</td>
<td>46,500</td>
<td>42,500</td>
<td>38,000</td>
<td>34,000</td>
<td></td>
</tr>
<tr>
<td>CMark/T thread</td>
<td>7,625</td>
<td>7,250</td>
<td>7,313</td>
<td>7,125</td>
<td>6,938</td>
<td>6,500</td>
<td>6,000</td>
<td>5,813</td>
<td>5,313</td>
<td>4,750</td>
<td>4,250</td>
<td></td>
</tr>
<tr>
<td><strong>T4240</strong></td>
<td></td>
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</tr>
<tr>
<td>CMark</td>
<td>179,763</td>
<td>179,763</td>
<td>179,763</td>
<td>179,763</td>
<td>179,763</td>
<td>179,763</td>
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<td>179,763</td>
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</tr>
<tr>
<td>CMark/T thread</td>
<td>7,490</td>
<td>7,490</td>
<td>7,490</td>
<td>7,490</td>
<td>7,490</td>
<td>7,490</td>
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</tr>
</tbody>
</table>
QorIQ RapidIO Manager (RMan)
T4240, T2080, P5040, P5020, P3041, B4860

• Dual Ports (Rev 2.1)
  - 1.25/2.5/3.125/5Gbs with x1/2/4 lanes
  - NWRITE/SWRITE/NREAD
  - Atomics
  - 34-bit Addressing
  - Large and small transport

• Supported Transaction Types
  - Type 9 Data Streaming
  - Type 10 Doorbells
  - Type 11 messaging
  - NWRITE/SWRITE
  - Port-write

• RMan Integrated
  - Support for hundreds of ingress/egress queues
  - Robust QoS
  - Non-CPU Ethernet - RapidIO bridging

RMan with RapidIO Switch Simplifies Virtualization
→ Off-load RDMA buffer copies between VMs – built in DMA/Messaging
→ Off-load lossless transmission – HW handshaked reliable transmission
→ Off-load transport protocol stack processing
→ Off-load Ethernet bridging and encapsulation
**RMan for QorIQ: Greater Performance and Functionality**

- Many queues allow multiple inbound/outbound queues per core
  - Hardware queue management via QorIQ Datapath Architecture (DPAA)
- Supports all messaging-style transaction types
  - Type 11 Messaging
  - Type 10 Doorbells
  - Type 9 Data Streaming
- Enables low overhead direct core-to-core communication

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**Device-to-Device Transport**

- **QorIQ or DSP**
  - Core
  - Core
  - Core
  - Core
  - 10G
  - SRIO

- **Channelized CPU-to-CPU transport**
  - Type 9 User PDU
  - MSG User PDU

- **QorIQ or DSP**
  - Core
  - Core
  - Core
  - Core
  - 10G
  - SRIO

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RMan Enables New Zero-CPU Overhead Use Models

Scalable Multicore System

Ethernet Bridging

- Channelized Inbound Enet-to-remote CPU transport
- Transparent bridging w/zero CPU intervention for multiple classified Enet streams
Big Data System Connectivity – 10 processors one hop away

40 G Rio to back plane

10 x 24 = 240 Vcores
RapidIO switching
Bandwidth = 500 Gbps
Zero CPU overhead for Ethernet packet forwarding
Scalable thru backplane switches
Processor to Processor Ethernet forwarding latency ~ uSeconds
Lower power and Lower cost than Ethernet switching

Sub-microsecond chip to chip latency!
Scaling Larger—60 Processors/720 Cores (all links 20G, 4 hop max distance between any two processors) – Redundant paths (16 switches)