Designing SOC/FPGA with SRIO Interface

“The IP enabled solutions provider”
The Mobiveil Team

**Leadership**

- Management with 25+ years experience in Semiconductor/Silicon IP/Systems software
- Previously founded **GDA Technologies, Inc** and grew to strong IP and Services group, 500+ engineers strong.
- Working on SRIO IP & Solutions since 2003

**Key differentiators**

Developed several key high speed serial interconnect IP blocks in the last 10+ years (PCI Express, Hyper Transport, Serial RapidIO, SPI4.2, DDR4/3, Flash Controllers etc)

Platforms/Solutions approach to services
Dependable scale and breadth
Alliances, Industry affiliations and partnerships

**Locations**

Headquarters in Milpitas, CA
India design centers: Chennai & Bangalore
Configurable & Feature Rich

Company Overview

Silicon IP Expertise

SRIO IP & VIP Offering

Services Offering

Summary

- Latency, Bandwidth, QOS
- Area, Link width, Frequency, Packaging
- Design, Implementation, Verification Effort
- Address all Features

Functionality
- Time to Market
- Cost
- Performance

Geometry
- 40/28nm
- 65nm
- 90nm
- .13u
- .15u

Data Rate
- Gen3
- Gen2
- Gen1

Technology
- COT
- ASIC
- Structured ASIC
- FPGA

Protocol
- SR-IOV & ARI
- PCIe-AMBA Bridge
- Switch
- AS
- EP+RC
- SW Port
- RC
- EP

Data path
- 256 bit
- 128 bit
- 64 bit
- 32 bit

Port width
- X32
- X16
- X8
- X4
- X1

Agenda
VIP Integration

- Exhaustively verified with many BFM/VIP
- Mobiveil provides Verification Test bench based on Customer VIP
  - Speeds up Chip level verification
  - All VIP Integration and setup issues are resolved upfront
Mobiveil IP Advantages

Market leading & most exhaustively proven cores in the market: Industry leaders are using these cores

Consortium Participation: RIO – Member, PCISIG – Member, HMC – Member, NVM Express - Member

Superior Technical Solution: Most Feature rich IP, Complete Customization and delivery Solution

Support: Clear IP Focus & Worldwide Support

3rd Party Partnerships for complete Solution: (Verification and PHY IPs)

Standard Body Certified Cores: All Mobiveil IPs are validated and certified: PCI Plug fest, UNH, RTA

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Summary
## RTL IP Portfolio

<table>
<thead>
<tr>
<th>IP Family</th>
<th>Product</th>
<th>Platinum (Proven in Silicon)</th>
<th>Gold (Proven in FPGA)</th>
<th>Under Development</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCI Express</td>
<td>Gen1</td>
<td>Y</td>
<td>Y</td>
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<td></td>
<td>Gen2</td>
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<td>Gen3</td>
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<td></td>
<td>Switch</td>
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<td>Y</td>
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<tr>
<td>SRI0</td>
<td>Gen1</td>
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<td>Gen2</td>
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<td>Gen3</td>
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<td>Ethernet</td>
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<td>10G &amp; HiGig</td>
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<td>DDR4/3</td>
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<td>Flash Controller</td>
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<td>eSDHC</td>
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<tr>
<td>SPI4.2</td>
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<tr>
<td>LPDDR3/2</td>
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<tr>
<td>NVM Express</td>
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<td></td>
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<tr>
<td>mPCIe/ HMC</td>
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</table>
Generic RapidIO Controller (GRIIO)
GRIO Architecture

- Highly Configurable
- Technology Independent
- System Validated

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Highlights

- Silicon IP used by many leading edge Base station Processors and ASICs
- Leverages Mobiveil’s high speed IO design expertise and market leadership
  - Supports all PHY specifications and data rates
  - Interoperability tested against the RTA BFM and test suites
  - System validation on FPGA platform
  - High performance, low gate count, low latency solution
  - Targets both FPGA and ASIC technologies
  - Support for mainstream technologies, tools and flows
  - Highly configurable design to optimize implementations
RapidIO to AXI Bridge (RAB)

- **Logical and Transport Layer**
- **Physical Layer**
- **sRIO SERDES Interface**
- **AXI Bridge (PIO, DMA, DME, DS)**
- **AXI Interface**

- **✓ Highly Configurable**
- **✓ Technology Independent**
- **✓ System Validated**
RapidIO Plan

- Mobiveil is working on 10xN (Gen3.0) Implementation
  - Added support for 10.3125 GBPS Baud rate
  - Use of 64/67b encode/decode as opposed to 8b/10b for Gen1/Gen2. Providing significant jump in data rate as overhead is much less compare to Gen1/Gen2.
  - Maintains backward compatibility for upper layers (Transport and logical layers).

- Mobiveil is part of Part S and NGSIS task force defining Next Generation Space Interconnect
  - Enhancements needed for Longer cable length
  - Enhancements needed for Error Management and reliability
  - Enhancement needed for possible Non-posted Multicasting

✓ Highly Configurable
✓ Technology Independent
✓ System Validated
RapidIO 10xN VIP Offering

- UVM based environment
- Extensive Compliance Test Suite
- Simplified Verification Flow and corresponding reduction in Chip Level Verification Effort
- Coverage Driven Constrained Random Verification
- Multiple levels of Verbosity for Easy Debug
- Comprehensive Traffic Tracking and Report Generation (Packet and Symbol level)
- Score Board
- Functional Coverage
- Protocol Monitor
ASIC Design Services

ASIC Services Offered
- ASIC/SoC design and verification – block level and chip level
- FPGA prototyping
- FPGA Validation

Resource Augmentation
- Skilled resources with design, verification and validation with varied domain expertise
- Resource deployment for short term/long term in APAC, Europe, North America

Offshore Development Center
- All round in house expertise (HW, SW) to independently manage design or verification effort
- Ability to quickly ramp up and provide a minimum risk execution model
P3041 AMC Card

Features:
- Single Width AMC card | Upto 4GB on-board DDR3 SDRAM
- Two Ethernet Interface in Face Plate | Optional GPS clock
- Dual SATA 2.0 Interface | Linux Operating System
- Virtual COM port for Debug | IPMI support for MMC – Pigeon Point
- sRIO and PCIe interfaces to backplane | Two CIPRI Interface in Face Plate
- Support Mezzanine Card interface with sRIO and CPRI interface for Baseband expansion

Target Application Areas
- Network Security
- Wireless
- Storage
SRIO Services Offering

• Team in Mobiveil has Expertise in building AMC boards for Wireless Base Stations with SRIO interconnects
  – P3041 Freescale Board with sRIO for DSP expansion
  – P2020 with MSC8156 add on board with sRIO Switch
  – Developed Faraday based DSP boards
  – MPC8540/MPC8560 based AMC board
  – MSC8122 and MSC7119 Freescale DSP for Voice Encoding

• Software
  – Modified open Source driver to integrate the SRIO configuration between Processor and DSP
  – Worked on Smart DSP OS (SDOS) from Freescale
  – Worked on Remote DMA and sRIO boot in MPC8540/8560
  – Provide Loopback function for Manufacturing diagnostics
  – 8122/7119 DSP configured for data movement using sRIO for Voice encoding in GSM base station
SRIO Services Offering

- SRIO Switching hub using IDT chipset
- Processing card with SRIO backplane (x86/ARM)
- Wireless Base station in AMC form factor
- Video Solutions with DSP form with Codec supports for Broadcast Segment
- FPGA based SRIO solutions for custom requirements
- Form factor – ATCA/AMC form factors
IP Enabled Solutions Provider

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- **Services Offering**
- **Summary**

**SRIO RTL IP**

- Test/validation
- Protocol Engineering

- BSP/Firmware
- SOC Design
- HW Design