<table>
<thead>
<tr>
<th>Time</th>
<th>Session Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9:00 am</td>
<td>Registration</td>
</tr>
<tr>
<td>10:00 am</td>
<td>RTA: RapidIO Intro, 10xN Specification launch and DCCN update</td>
</tr>
<tr>
<td>10:45 am</td>
<td>Freescale Solutions with RapidIO</td>
</tr>
<tr>
<td>11:15 am</td>
<td>Fabric Embedded Tools Software for RapidIO Networks</td>
</tr>
<tr>
<td>11:45 am</td>
<td>Technical Demo</td>
</tr>
<tr>
<td>12:15 pm</td>
<td>Lunch</td>
</tr>
<tr>
<td>1:30 pm</td>
<td>Prodrive: Enabling Advanced Applications with RapidIO</td>
</tr>
<tr>
<td>2:00 pm</td>
<td>IDT: RapidIO for Low Latency Servers and Wireless Base Station</td>
</tr>
<tr>
<td>2:30 pm</td>
<td>Break</td>
</tr>
<tr>
<td>2:45 pm</td>
<td>Mobiveil: Designing SOC/FPGA with S-RIO Interface</td>
</tr>
<tr>
<td>3:15 pm</td>
<td>Texas Instruments Multi-core Processors with RapidIO</td>
</tr>
<tr>
<td>3:45 pm</td>
<td>Wrap-up and Networking</td>
</tr>
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</table>
RTA Presentation Agenda

- RapidIO Intro
- Ecosystem and Protocol Attributes
- RapidIO 10xN Specification Overview
- RapidIO Data Center Compute and Networking Update
- RapidIO in SDN/Openflow
RapidIO’s Value Proposition

- A Multi-Processor Embedded Interconnect
- A **Disruptive Architecture**, that changes the basic economics of deployment in all multi-processor applications
- A **Mature** technology – 10 years of market deployments
- Designed for the unique requirements of **embedded processing and communications systems**
- A **scalable** solutions for board, backplane and inter-chassis communication
- Offers **lowest overall system power**
- Provides superior **end to end packet latency**, throughput and fault tolerance
- Offers **flexibility** to support evolving system configurations, even in the field

Over 6 million switches shipped
Other Defining Attributes

- Reliability
- Determinism
- Power Efficiency
- Latency
- System Topology
- Cost
RapidIO Interconnect combines the best attributes of PCIe and Ethernet in a multi-processor fabric.
Comparison

OSI Layer

Layer 1: Physical
- 10/100/100 Base-T

Layer 2: Data Link
- Ethernet

Layer 3: Network
- IP

Layer 4: Transport
- TCP
- UDP
- Custom

Layer 5+: Application
- RDMA
- Custom

Ethernet

RapidIO

Software Hardware

- Read, Write, Messaging, Datagram, Encapsulation
- Transport Layer
- Reliable Delivery
- LP-LVDS
- LP-Serial
Major Recent RapidIO News

- RapidIO based Supercomputer Launched with 2x Gflops per watt vs. top computer in Green 500
- Launch of RTA DCCN Initiative, press and EEtimes coverage
- RapidIO based data center computing presented at facebook OCP Summit Aug
- Early traction in Super Computing and Server markets, launch of Browndwarf Supercomputer with TI ARM + DSP
- IDT presents x86 Supercomputing platform at Intel Developer Forum Sep 2013
- DCCN first draft reference design presented at Open Server Summit in Santa Clara
Wireless topologies: moving to Data Center and HPC

Computing Topologies: 20 – 100 Gbps
- Micro Server
- Super computers
- Blade server
- Storage

Embedded Topologies Up to 20 Gbps
- Wireless Base Station
- Video Conferencing
- Imaging
- Mil / Aero
RapidIO 10xN Specification
RapidIO 10xN Overview

3rd Generation
Scalable embedded
peer to peer
Multi processor
Interconnect
On board, board-to-board and
Chassis to Chassis

- S-RIO 10xN: data rate of 40-160 Gbps per port
- 10.3125 Gbaud per serial lane with option of going to 12.5 Gbaud in future
- Long-reach support (100 cm through two connectors), Short Reach 20 cm 1 connector, 30 cm no connector
- Backward compatibility with RapidIO Gen2 switches (5 & 6.25 Gbps) and endpoints
- Lane widths of x1, x2, x4, x8, x16
- Speed granularity from 1.25, 2.5, 3.125, 5, 6.25, 10.3125 Gbaud

Key Additional Features
- 10 Gbps per lane
- 10 to 160 Gbps per port
- 64/67 encoding
- Power management
- Time Distribution
RapidIO 10xN to 25xN Highlights

- Builds on deployment of over 30 M 10-20 Gbps RapidIO Ports
  - > 6M switches shipped
  - exceeds 10 GbE port shipments in 2012

- 10Gbps/lane silicon development
- 25Gbps/lane next gen backplane switches

- PCIe3 NIC to RapidIO 10xN
- RapidIO Endpoint IP (10xN) for ASICs

- Large Ecosystem of software support
  - Linux, Windows, VxWorks
  - Boards and Debug Software
RapidIO 10xN Spec New Functionality

Physical Layer Enhancements
  – Electrical specifications
  – Information Encoding Scheme
  – Link Initialization
  – Ordered Sequences
  – Packet Exchange Optimizations
  – Time Distribution

Transport Layer Enhancements
  – Routing Table Programming Model
  – Add 32-bit Device IDs

Logical Layer: Unchanged

Standardization of Hot Swap Support
<table>
<thead>
<tr>
<th>Feature</th>
<th>2.X</th>
<th>10xN</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logical Layer</td>
<td></td>
<td><strong>Unchanged</strong></td>
<td>Protect previous logical layer investment</td>
</tr>
<tr>
<td>Transport Layer</td>
<td>• 8 and 16 bit Device IDs</td>
<td>• Add 32 bit Device IDs and new routing table programming model</td>
<td>Support more device</td>
</tr>
<tr>
<td>Physical Layer</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Port Widths</td>
<td>• 1, 2, 4, 8, 16 lanes</td>
<td>• Add Optional asymmetric link support</td>
<td>Save power</td>
</tr>
<tr>
<td>Lane Speeds</td>
<td>• 1.25, 2.5, 3.125, 5, 6.25 Gbaud</td>
<td>• Add 10.3125 Gbaud</td>
<td>Double the bandwidth</td>
</tr>
<tr>
<td>Electrical</td>
<td>• XAUI or OIF CEI 6 Gbaud</td>
<td>• Add IEEE 802.3 10GBASE-KR (802.3-ap, 802.3-ba)</td>
<td>Same as Ether electrical specification</td>
</tr>
<tr>
<td>Standards</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Encoding</td>
<td>• 8B/10B</td>
<td>• 64B/67B</td>
<td>Make encoding 20% more efficient</td>
</tr>
<tr>
<td>Information</td>
<td>• IDLE1, IDLE2</td>
<td>• Add IDLE3 and Ordered Sequences</td>
<td></td>
</tr>
<tr>
<td>Exchanged</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Other</td>
<td>• Packet exchange optimization</td>
<td></td>
<td>Reduce latency during error recovery and reduce the number of control symbols sent</td>
</tr>
<tr>
<td></td>
<td>• Add Time distribution</td>
<td></td>
<td>Determine the transmission delay</td>
</tr>
<tr>
<td></td>
<td>• Standard hot swap support</td>
<td></td>
<td>Easier to support hot swap</td>
</tr>
</tbody>
</table>
## RapidIO 10xN Electrical Specifications

<table>
<thead>
<tr>
<th>Feature</th>
<th>10GBASE-KR (802.3ap)</th>
<th>10GBASE-KR (802.3ba)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lane speed</td>
<td>10.3125 GBaud</td>
<td>10.3125 GBaud</td>
</tr>
<tr>
<td>Channel</td>
<td>10GBASE-KR channel, Annex 69A</td>
<td>Annex 83A.4, IEEE 802.3ba-2010</td>
</tr>
<tr>
<td></td>
<td>IEEE Standard 802.3-2008</td>
<td>IEEE 802.3ba-2010</td>
</tr>
<tr>
<td>PHY</td>
<td>72.6.1, 72.7.1 -72.9.5 IEEE 802.3-2008</td>
<td>Annex 83A.3 IEEE 802.3ba-2010</td>
</tr>
<tr>
<td>Reach</td>
<td>1 meter of copper PLUS 2 connectors</td>
<td>20 cm of copper PLUS 1 connector</td>
</tr>
<tr>
<td>Bit Error Rate</td>
<td>$10^{-15}$</td>
<td>$10^{-15}$</td>
</tr>
</tbody>
</table>

RapidIO 10xN is based on industry standard Ethernet electrical specifications.
10xN Information Encoding Scheme

Maintain DC Balance

“Type 0” Control Codeword

“Type 1” Data Codeword

Packets

Control Codewords

Control Symbols
### 10xN Packet Exchange Optimizations

<table>
<thead>
<tr>
<th></th>
<th>2.x Single Acknowledgement</th>
<th>3.0 Multiple Acknowledgement</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>One Packet Accepted</strong></td>
<td>One Packet Accepted sent for each Packet</td>
<td>Single “Packet Accepted” can acknowledge up to XXX packets</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>2.x Error Recovery</th>
<th>3.0 Error Recovery</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Packet transmission resumes after Packet Not Accepted, Link-Request, and Link Response Control Symbols</strong></td>
<td>Packet transmission resumes immediately after the Link Request Control Symbols.</td>
<td></td>
</tr>
</tbody>
</table>
Calibrating Transmission Delay

System Time Distribution

RapidIO Switch

System Time Master

Slave Port

Device Time

Master Port

System Time Slave

TSG Master

Send Loop-Timing Request

Process Loop-Response

Compute Loop Delay

Set Timestamp Offset

Set Slave TSG

TSG Slave

Loop-Timing Request

Loop-Response With Delay

Delay

Send Timestamp Control Symbols

Time Synchronization Protocol
Routing Table Programming Model

- Hierarchical programming model
- Supports 32, 16, and 8 bit DevIDs
- Each entry routes packets to:
  - Egress port number
  - Multicast mask number
  - Group number for next lower level
  - Use default route
  - Discard this packet
Data Center Compute and Networking

RapidIO

Multi-Processor
Embedded Interconnect

Switched | Scalable | Low Latency | Reliable

10 Gbps  20 Gbps  40 Gbps  100+ Gbps

ANY TOPOLOGY
ANY PROCESSOR
OPEN STANDARD

WIRELESS INFRASTRUCTURE | SERVER | HPEC | IMAGING | AEROSPACE | INDUSTRIAL
RapidIO Data Center Initiatives

- **Data Center Compute and Networking task group** = DCCN
- **Task group** being set up inside the RTA to drive collaborative development of RapidIO reference designs to target data center organizations:
  - OCP,
  - Scorpio,
  - Financial Data Center,
  - Super computer
- Reference designs for Compute/Motherboard and Networking/Switching
- Open Industry wide collaboration with several semiconductor, software and board/systems vendors participating
- **Goal:**
- Release Phase 1 spec’s in 2H 2013 *(draft announced at Open Server Summit)*
- Phase 1 = functionality optimized CPU agnostic compute/motherboards
- Phase 2 = performance, density, power optimized CPU agnostic compute/motherboards
CPU Agnostic RapidIO 20 Gbps Motherboards

- Compute Nodes with x86 use PCIe to S-RIO NIC
- Compute Nodes with ARM have native RapidIO endpoints
- DSP for compute intensive applications
- Up to 20 Gbps per link
- Ultra low latency
- Scales to 64k nodes
- 100 ns switch latency
- Storage solutions in development

![Diagram of CPU Agnostic RapidIO 20 Gbps Motherboards]
PHASE 1:

- Mechanical and Electrical form factors ideally useable by OCP
- Re use existing RapidIO Processor ecosystem of AMC/Daughtercards
- Base Motherboard with connectors for AMC/daugthercards
- Compute Nodes with x86 use PCIe to S-RIO NIC on Daughtercard
- Compute Node with ARM/PPC/DSP/FPGA are native RapidIO connected with small switching option on card
- DSP for compute intensive applications
- Up to 20 Gbps per link
- Small RapidIO switch per base card
- 20-40 Gbps RapidIO links to backplane and front panel for cabling
- 10 GbE added for ease of migration
- Local switching card/s will have similar form factor to Computer/Motherboards
Phase 1 Rendering

- Availability Q1 2014: Processor Agnostic Phase 1 RapidIO Motherboard
Phase 2: CPU Agnostic RapidIO 20 Gbps Motherboards

- Mechanical and Electrical form factors ideally useable by OCP
- Cost, Density, and Power Optimized
- More processing capacity per motherboard
- Remove daughtercards and connectors from phase 1
- Compute Nodes with x86 use PCIe to S-RIO NIC on motherboard
- Compute Node with ARM/PPC/DSP are native RapidIO connected with small switching option on motherboard
- Up to 20 Gbps per link
- Small RapidIO switch per base card
- 20-40 Gbps RapidIO links to backplane and front panel for cabling
- Local switching card/s will have similar form factor to Computer/Motherboards
- Interoperable with Phase 1 cards

Density, Power and Cost Optimized
20 Gbps Data Center Scaling

- Switching at board, chassis, rack and top of rack level
- Scalability to 64K nodes, roadmap to 4 billion
- Application focus
  - Latency sensitive analytics
  - Financial
  - High-Performance Computing (HPC)
- Proven in Telecom, Medical, Industrial

2x Performance per port of 10GigE top of Rack
OpenFlow Using RapidIO Fabrics
RapidIO as an OpenFlow Fabric

- RapidIO Fabric
- OPENFLOW SWITCH
- Application
- Processor
- Open Flow Switch Port/RapidIO Port
- Open Flow Switch Port/RapidIO Port
- Open Flow Switch Port/RapidIO Port
- Open Flow Switch Port/RapidIO Port
- SDN/OpenFlow Controller
- Application
- Processor
- Application
- Processor
OpenFlow Switch Platform Concept

OpenFlow Switch Box
(Communications Gateway)

OpenFlow Switch Cluster
(Data Center Applications)
Value of RapidIO for OpenFlow

- Low, deterministic latency
- Guaranteed, in order packet delivery
- QoS mechanisms support OpenFlow
- In-band, scalable, highly accurate hardware time-distribution to support timeouts
- Scales to thousands of ports in a single “logical” OpenFlow switch
- Supports fault tolerant operation
Summary

- RapidIO for Multi Processor Systems
- 3 layer protocol terminated in hardware, no TCP Offload needed
- 30 million RapidIO Ports @ 10-20 Gbps deployed
- 100ns cut through latency
- Sub microsecond end to end packet termination
- Highest Gflops per watts with Green 500 ready product launch (6.4 Gflops per watt)
- Building on Supercomputing, Servers and Data Center
- RapidIO 10xN Spec Launched, with 40 Gbps per x4 port with big power and efficiency gains over Gen2
- RTA Data Center Group kicked off to start new reference designs.
- RapidIO looking into initiative for Openflow/SDN

Thank you for joining RTA Global Design Summits Asia 2013