

RapidIO Gen2 Keeps Pace with Evolving Wireless Standards

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Since LTE has been accepted as a 4G technology by the International Telecom Union (ITU) and commercial LTE becomes reality, the standard is now mature enough for silicon vendors to begin the commoditisation of LTE System-on-Chip (SoC) devices. Does this mean that multi-processor wireless solutions still have a future? And do we still need a high-speed interconnect? In our view, it's a clear yes to both questions.

Although higher-performance, more specialised SoC devices are being launched daily they belong in the femtocell and picocell markets: they are not designed to address macrocells and wireless test equipment. Also, the 3GPP standards are not about to stop developing. Release 10, LTE-Advanced (LTE-A), is expected to be finalized in March 2011 and will pave the way for the first release of the ITU Radio communication sector's (ITU-R) IMT-Advanced – a global platform for interactive mobile services. This is also coupled with the demand for improved signal coverage and efficiency leading to 8x8 MIMO requirements and beam forming capabilities.

In these scenarios, the resulting data bandwidth and diversity requirements mean that a multi-processor solution should be considered as an option that can deliver the right level of processing power at the right cost points. This in turn drives the need for an interconnect to link the processors together, both chip-to-chip and card-to-card across a backplane. Embedded applications typically have three overarching requirements: low-cost; common, re-usable components; and standards based interfaces. Together these achieve a high system performance.

About SRIO

Serial RapidIO (SRIO) has proven itself to be the interconnect of choice for this type of multi-processor system. It provides an excellent combination of low cost, low power, high throughput and advanced features. SRIO has a lower protocol overhead compared to Ethernet, can have multiple masters unlike PCI Express, and supports multicast. It has better flow control mechanisms than Ethernet, allowing a higher utilisation of raw bandwidth.

SRIO is a good example of a modern interconnect. Originally developed as a processor interconnect, SRIO is suitable for both control and data. It is a point-to-point packetized architecture that can support arbitrary topologies, with low overhead. It allows for variable packet size, with a maximum 256 byte protocol data unit (PDU).

As well as its high throughput, SRIO is also an efficient technology to implement. It inherently supports carrier-grade quality of service (QoS), whereas Ethernet requires an additional protocol layer and network co-operation. This gives SRIO a cost and power advantage over Ethernet (per volume of data). Since features are typically handled by a SRIO peripheral on the target device, data transfer has no impact on the performance of the target processor.

SRIO Gen2

Responding to increased requirements such as these, RapidIO Gen2 provides the necessary step-change in deployable technology to double the effective bandwidth of SRIO links, improve link flexibility, and introduce traffic measurement. It was ratified in October 2009 by the RapidIO Trade Association, and products using SRIO Gen2 are now available for system designers to use.

At the physical layer, new 5Gbaud and 6.25Gbaud lane rates allow a 4x link to achieve a usable bandwidth of up to 20Gbps, while 2x and 8x link options increase the connection flexibility. Differential Feedback Equalization ensures that the faster links maintain the same bit error rates as Gen1 connections.

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The RapidIO Gen2 logical layer is backwardly compatible with Gen1. DirectIO, mailboxes, doorbells, multicast and streaming are all supported. However, Gen2 also introduces Traffic Management (TM) packets which allow the network to react to congestion and increase the effective link bandwidth. TM allows a SRIO traffic consumer to throttle back a traffic generator which is overflowing its data buffer, allowing other generators to get a share of the resource.

Generally, for embedded systems, alternative technologies to SRIO Gen2 include 10Gigabit Ethernet, which is a well-known and reliable choice and hence perceived as low risk, and PCI Express Gen2, which is perhaps best suited to PC and server applications. SRIO has significant advantages as a system interconnect in its QoS and flow control features, its support for arbitrary topologies, and its low overhead with minimal silicon footprint.

Wireless baseband processing

Let's consider wireless baseband processing as an example of a high-performance multi-processor application. A blade-level subsystem solution may include both DSPs and FPGAs, with the mix being selected to suit the requirements of the particular application. The CommAgility AMC-2C6670 AdvancedMC module, for example, includes two Texas Instruments (TI) TMS320C6670 DSPs, each with four 1.2GHz C66x cores, as well as a Xilinx Virtex-6 LX240T FPGA. A SRIO Gen2 fabric, based around the IDT CPS-1848 SRIO switch, is used for radio data distribution and as a low-latency direct memory access between devices, both on- and off-card.

Using SRIO for both intra- and inter-card connectivity allows the various elements to be brought together: the AMC-2C6670 provides two or three high-speed 20Gbps links on and off the card using a 4x SRIO interface, offering the deterministic bandwidth required. A separate three link full-duplex 6.144Gbps CPRI/OBSAI compliant antenna interface, with configurable clocking and synchronisation, provides additional interface capabilities targeted to wireless radios. An AMC.2 Gigabit Ethernet link is provided for OA&M and transport of processed data streams.

Macro Basestations

To achieve the 1Gbps peak data rate required by the ITU, LTE-A requires more backplane bandwidth. A complete 70-MHz, 4-antenna, 3-sector solution must be implemented using the multiple DSPs across multiple modules. The IDT SRIO switch is used to accommodate the FPGA on the module, which performs the LTE-A acceleration not supported by today's SoCs. The C6670 improves the cost and power per channel by accelerating key components of baseband processing such as matrix math processing. The same architecture could be leveraged for pico and microcell coverage.

In macro base stations, SRIO can be used to move digital "chip rate" data from the multiple subscriber antennae to the multiple baseband processing cards in the system. Each baseband card includes a SRIO interconnect and would typically be based around a high-performance DSP SoC supporting SRIO, such as a TI C6670. The data processed by the baseband cards is then forwarded to the backhaul interface, which can also be over SRIO.

In either an ATCA or MicroTCA chassis system, using SRIO as the primary data transport gives integrators the option of mixing and matching DSP-centric and FPGA-centric blades to get the right balance of technology. The AMC.4 specification supports the 20Gbps 4x SRIO links across the chassis backplane between cards. Companies such as Texas Instruments, IDT, and Freescale Semiconductor have played an important role in promoting SRIO and ensuring its maturation. Multiple vendors now provide SRIO support for both MicroTCA Carrier Hubs, and control and signal processing AMC cards.