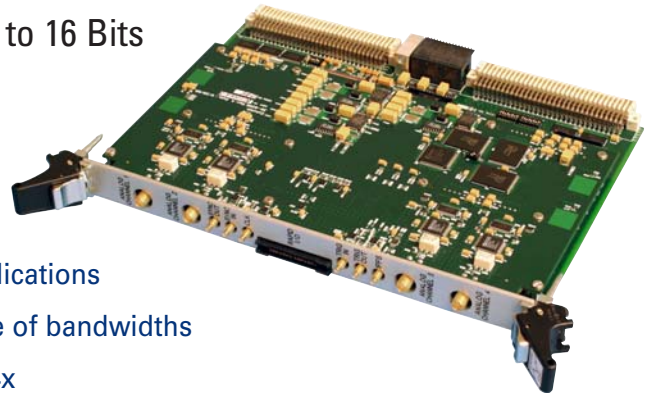


ECV4-4 Four-Channel, Wideband, FPGA-Based Digital Receivers

High-Speed A/D Conversion, Resolution from 8 Bits to 16 Bits

- Massive processing power from seven user-programmable Virtex™-4 FPGAs plus one Stratix® FPGA
- Optimized for composite, multi-channel data processing in beam-forming and direction-finding
- Well suited to COMINT, Telecommunications, and Radar applications
- Flexible architecture allows the family to cover a wide range of bandwidths
- Multiple backplane interfaces for VXS, RACE++®, and VME64x



The Echotek™ Series ECV4-4 family of digital receivers from Mercury Computer Systems implements a flexible baseboard plus mezzanine architecture while supporting an extremely high density of FPGA-processing power. This combination of flexibility and power allows the family to deliver unique capabilities, such as multi-board coherency, while addressing a range of analog signal requirements.

Analog Flexibility via Mezzanine Options

Each member of the ECV4-4 family consists of a unique analog mezzanine card coupled with a common FPGA-based digital baseboard. The mezzanine card determines the analog I/O connectivity and functionality. Each mezzanine card is configured with a specific set of A/D and/or D/A converters addressing a defined bandwidth and frequency for data conversion. Some mezzanines have four A/D converters, some have two, while others have a combination of A/Ds and D/As, so the board operates as a transceiver. The mezzanine card also includes various clocking and synchronization inputs and outputs, as well as up to 256 MB of Flash memory.

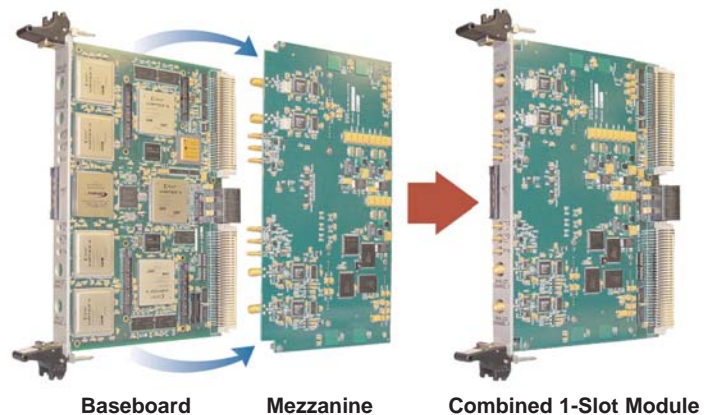
Processing Power from 8 FPGAs on Baseboard

The baseboard is common to all members of the ECV4-4 product family and supports a powerful set of FPGAs. Four Xilinx Virtex™-4 SX FPGAs function as channelizers, while two Virtex-4 FX FPGAs operate as cross-channel processors. These FPGAs allow the user to run custom algorithms such as digital down/up conversion (wideband or narrow-band), fast Fourier transforms (FFT), and filtering directly on the board. A third Virtex-4 FX FPGA is dedicated to board control and backplane I/O, while an Altera Stratix® EP1S FPGA manages a high-speed RapidIO® front-panel interface used to facilitate simultaneous processing of data from two separate boards. In support of the FPGA processing power, the board also includes up to 1 GB of DDR SDRAM and 4 MB of DDR-II SRAM.

Architected for Beam-Forming and Direction-Finding

The architecture of the ECV4-4 is optimized to support composite, multi-channel data processing for beam-forming and direction-finding. On the baseboard, a set of four Virtex-4 SX FPGAs serve as the first level of interface to the A/D (or D/A) converters on the mezzanine. These four FPGAs function as wideband digital receivers/transmitters and then move channelized data to or from three FPGAs at the next level of the architecture. At this level are two Virtex-4 FX FPGAs, the cross-channel processors. These FPGAs can manipulate data from any of the four channels simultaneously, delivering coherent processing of multiple data streams.

Also at the level of the cross-channel processors is a Stratix EP1S FPGA, which functions as a data transfer processor in 2-board configurations. This data transfer processor uses a full-duplex 16-bit parallel RapidIO link to provide a real-time, deterministic connection between two ECV4-4 boards, enabling channelized data packets acquired from either of the two boards to be processed simultaneously. The RapidIO link operates at 1 GB/s in both directions simultaneously, enabling coherent processing of up to eight channels of data across two modules.



Unique Application Suitability

A common challenge in SIGINT, Radar, and Air Traffic Control applications is to get wideband data from eight antenna elements to the same place at the same time for beam-forming. The ECV4-4 product addresses this challenge well, because two boards can combine data to achieve simultaneous and coherent access to eight individual inputs. This special capability is delivered by the ECV4-4 family in only two VME slots.

Backplane I/O

The final level of FPGA processing is a single Virtex-4 FX that functions as the board controller and also manages backplane I/O. This FPGA provides a fully compliant VME64 interface to the P1 and P2 connectors via the Tundra® Universe™ integrated circuit. In the current configurations, these products use the VMEbus exclusively for command and control, and consequently support only single-cycle VMEbus reads and writes.

In addition to classic VME support, multiple additional options are available within the ECV4-4 family. One option provides two RACE++® (VITA 5.1-1999) interfaces, transferring packet data over the RACE++ switch fabric. The RACE++ bandwidth is 264 MB/s on each connection for a total of 528 MB/s.

Some members of the ECV4-4 family provide 4x serial connectivity to the VXS (VITA 41) P0 connector. Each serial link is capable of running up to 2.5 Gb/s in each direction, for a total of 10 Gb/s for

the 4x link. This equates to an effective bandwidth of 1 GB/s for the VXS link in both directions. Other members of the ECV4-4 family provide a VME64x P0 connector for signaling and control.

Data Links

The Virtex-4 FPGAs on the baseboard are interconnected by multiple high-speed data link connections that can run up to 400 MB/s for 4-bit connections and 800 MB/s for 8-bit connections. In addition, data links interconnect selected FPGAs with DDR SDRAM and DDR-II SRAM.

The block diagram in Figure 1 shows the multiple data links. The type, speed, and configuration of each data link are defined in the color key that accompanies the figure.

Market-Leading Signal Integrity

Echotek products deliver the finest signal integrity, measured by SNR (signal to noise ratio) or SFDR (spurious free dynamic range).

Options to Fit a Range of Applications

The ECV4-4 family offers a range of options to address a variety of application requirements. The models are listed in the following table.

ECV4-4 Models

Model	Data Inputs/Outputs	Data Conversion	P0 Connector
ECV4-4-R105-VME64X	4 AC coupled inputs	14-bit 105 MHz A/D	VME64x
ECV4-4-R105-VXS	4 AC coupled inputs	14-bit 105 MHz A/D	VXS
ECV4-4-R1500-VME64X	4 AC coupled inputs	8-bit 1.5 GHz A/D	VME64x
ECV4-4-R1500-VXS	4 AC coupled inputs	8-bit 1.5 GHz A/D	VXS
ECV4-4-R210-VME64X	4 AC coupled inputs	12-bit 210 MHz A/D	VME64x
ECV4-4-R210-VXS	4 AC coupled inputs	12-bit 210 MHz A/D	VXS
ECV4-4-3R105-1T400-VME64X	3 AC coupled inputs / 1 AC coupled output	14-bit 105 MHz A/D/ 14-bit 400 Hz D/A	VME64x
ECV4-4-3R105-1T400-VXS	3 AC coupled inputs / 1 AC coupled output	14-bit 105 MHz A/D/ 14-bit 400 Hz D/A	VXS

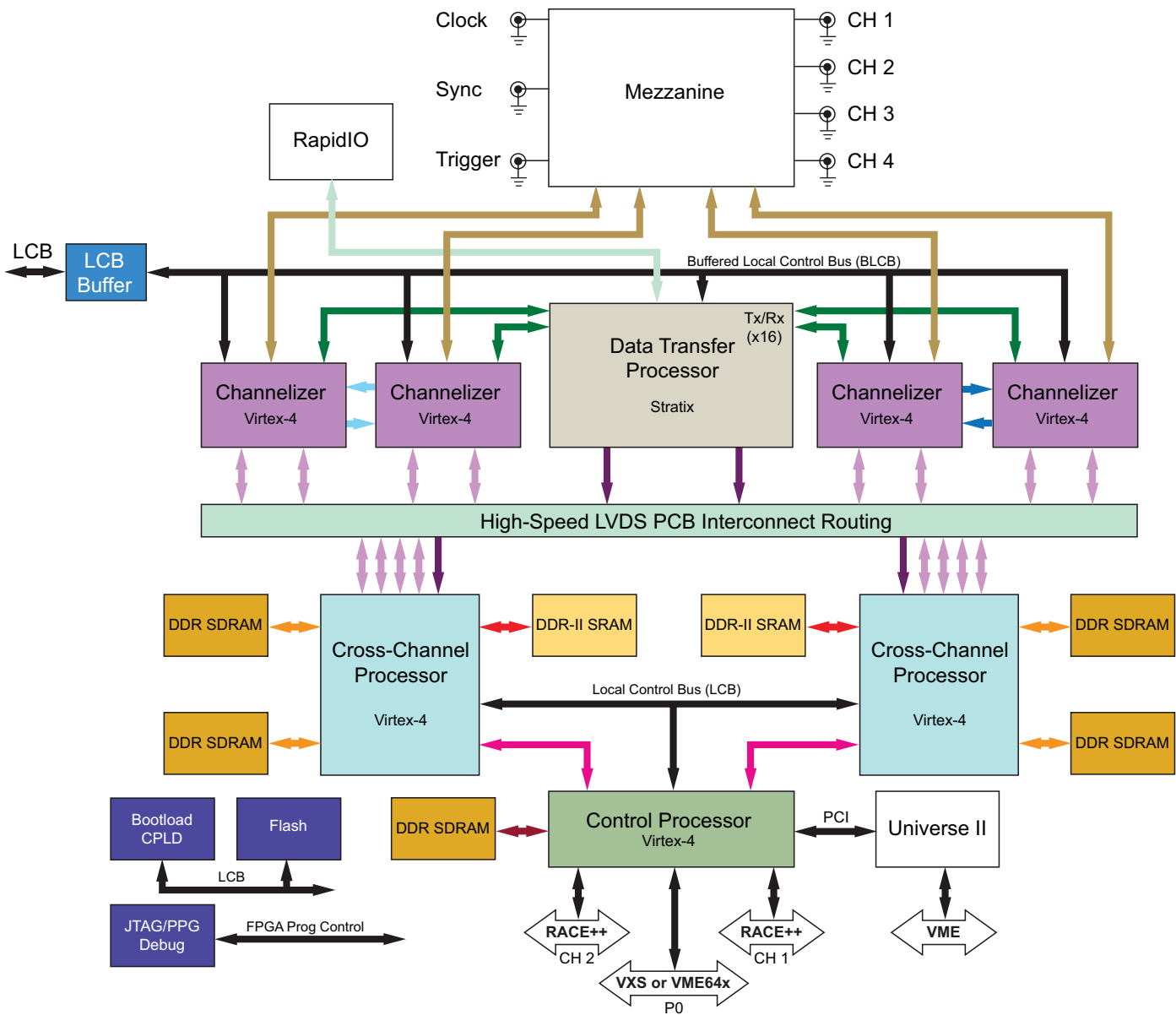


Figure 1. ECV4-4 Block Diagram

Data Links

Link	Type	Speed	Configuration
User-specific Cross-Channel Processor to/from Control Processor	LVDS	800 MB/s	Full-duplex
User-specific Cross-Channel Processor from Data Transfer Processor	LVDS	800 MB/s	Half-duplex
User-specific Cross-Channel Processor to/from Channelizer	LVDS	400 MB/s	Full-duplex
Channelizer 1 to/from Channelizer 2	LVDS	800 MB/s	Full-duplex
Channelizer 3 to/from Channelizer 4	LVDS	800 MB/s	Full-duplex
RapidIO port to/from Data Transfer Processor	LVDS	1.056 GB/s	Full-duplex
Mezzanine to/from Channelizer	Mezzanine-specific	Up to 1.6 GB/s	Half-duplex (direction configurable)
Channelizer to/from Data Transfer Processor	LVTTTL	532 MB/s	Half-duplex (direction configurable)
User-specific Cross-Channel Processor to/from DDR SDRAM	SSTL	1.336 GB/s	x32
User-specific Cross-Channel Processor to/from DDR-II SRAM	HSTL	2 GB/s	x32
Control Processor to/from DDR SDRAM	SSTL	800 MB/s	x32

Specifications

FPGAs

Virtex-4 FPGAs

7 FPGAs total	2,496 XtremeDSP slices 40,752 Kb of block RAM 467,656 logic cells
4 channelizers	Xilinx Virtex-4 XC4VSX55
2 cross-channel processors	Xilinx Virtex-4 XC4VFX60 or XC4VFX100
1 control processor	Xilinx Virtex-4 XC4VFX60 or XC4VFX100 Supports VxWorks accessible via TCP/IP over the VME connector

Stratix FPGA

1 data transfer processor	Altera Stratix EP1S60
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Memory

DDR SDRAM	128 MB with 32M x 32-bit chips or 256 MB with 64M x 32-bit chips
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DDR-II SRAM	2 MB with 512K x 32-bit chips
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Flash	128 MB with 128M x 8-bit chips
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Environmental

Ruggedization level	Commercial
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Temperature

Operating	0°C to 55°C with 300 ft/s appropriate airflow
Storage	-50°C to +85°C

Vibration	0.002g ² /Hz from 10 Hz to 2000 Hz random 2g sinusoidal from 5 Hz to 500 Hz
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Shock	20g peak sawtooth, 11 ms duration
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Humidity	Up to 95% RH
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Cooling	Commercial grade, cooled by blown air, for use in benign environments and software development applications
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