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RapidIO Interworking to Cover a Broad Base of Applications!

By Tom Cox

Executive Director

RapidIO Trade Association



The value proposition of the RapidIO interconnect technology has commanded the attention of a wide range of embedded markets, each for the unique and varied features defined by the standard that are available in the hundreds of RapidIO-based products in the marketplace. A common element in all of these systems is the requirement to interwork with other interconnect technologies – both legacy and new, equally proprietary and industry standard.

From its very first inception, RapidIO technology has embraced interworking with other protocols and interconnects. For example, PCI load store operations are at the root of the RapidIO memory mapped IO architecture. In addition, the full-featured message passing and maintenance protocol can support Ethernet and other capabilities. By design, translating from one interconnect's language to another is performed easily in hardware with specifically designed end-points or with the support of embedded processors.

In storage applications we see RapidIO and PCI, PCI-X, and PCI-Express seamlessly interworking. RapidIO provides the backplane architecture and PCI is integrated into the endpoints. RapidIO interworks equally well with out-of-the-box interconnects in storage systems such as Infiniband or Fibre Channel. In many highly fault-tolerant applications like large storage networks, reliable, high-speed data delivery is provided by RapidIO solutions.



Legacy interconnects that are well-established in proprietary OEM systems are often required in some form or another in new architectures and designs. When this is the case OEM's utilize ASIC and FPGA technology based on RapidIO cores and IP to develop interworking solutions to bridge the old to the new effortlessly.

RapidIO is an established, scalable, open-standard, switched fabric, designed by the leaders in embedded computing specifically for OEMs building equipment in the wireless infrastructure, edge networking, storage, scientific, military and industrial markets. RapidIO technology delivers the reliability, cost effectiveness, performance and scalability required in these markets. RapidIO also supports a roadmap which is attuned to the changes affecting designers of embedded infrastructure. RapidIO covers a broad base of interesting and exciting applications which include many different protocols and interconnects, and the possibilities are endless!

As the Executive Director of the RapidIO Trade Association I continue to see examples of RapidIO in action, and love to hear and learn more about applications of all types. Your examples would be most welcome! Simply send me an email (tom.cox@RapidIO.org) that describes your favorite illustration of RapidIO in action!

RapidIO Trade Association Announces Details of August 2006, Boston Global RapidIO Design Summit

Eco-system members join to present the latest products, application and standard developments in an informative, easy-to-join forum.

Engineering managers, system architects, and embedded product developers are invited to attend the RapidIO Trade Association's Boston Global RapidIO Design Summit to be held August 17th, from 9:00 a.m. to 5:30 p.m. at the Woburn Plaza Hotel. The Summit will provide valuable information on RapidIO technology and products and include working demonstrations in the technology lab. Sessions, application papers and design tips will be presented by RapidIO Trade Association members including Fabric Embedded Tools Corporation (FET), Freescale Semiconductor, FuturePlus Systems, Integrated Device Technology (IDT), Jennic, Mercury Computer Systems, Texas Instruments, Tundra Semiconductor Corporation, and Xilinx.

"This extraordinary Design Summit is structured to aid the embedded design community in learning how to get better system performance, reliability and support for convergence by using the high-speed, flexible RapidIO interconnect and fabric," said Tom Cox, executive director of the RapidIO Trade Association.

The free, full-day event includes a track of technical sessions highlighting RapidIO technology, interconnect comparisons, software considerations, RapidIO and distributed processing, wireless application design, and RapidIO products. In addition, a technology lab will feature multi-vendor RapidIO interoperability



demonstrations using state-of-the-art RapidIO products. Complimentary light breakfast, lunch and snacks will be provided.

All attendees will be entered in prize drawings for copies of *RapidIO: The Next Generation Communication Fabric for Embedded Application*, the definitive reference book (one for every 20 registered attendees) and the grand prize of an iPod nano. Attendees must be present to win. Space is limited and attendees are encouraged to register prior to August 8th. For general questions and more information, contact Sue Leininger, 512.305.0070. For registration details visit www.RapidIO.org/events/design_summits_2006/designsummit2006/.

In addition to the Boston event, Global RapidIO Design Summits have been scheduled throughout Asia-Pacific this Fall. Details can be found on www.RapidIO.org.

Hosted by the RapidIO Trade Association, the 2006 Global RapidIO Design Summits are sponsored by Altera, AMCC, EMC, ENEA, Ericsson, Freescale Semiconductor, Lucent Technologies, Mercury Computer Systems, Micro Memory, MontaVista, PMC-Sierra, Rydal, Texas Instruments, Tundra Semiconductor Corporation, Wind River, and Xilinx.

RapidIO Trade Association and OpenSystems Publishing Team to Sponsor RapidIO Webcast

Eco-system members Freescale Semiconductor, IDT, Mercury Computer Systems, and Tundra Semiconductor Corporation to discuss the latest product, application and standard developments.

The RapidIO Trade Association and OpenSystems Publishing (OSP) are teaming up to sponsor a webcast covering the latest RapidIO technology advancements and specification updates. The event, "RapidIO System Architecture: What Designers Need to Know," will be held August 24, 2006 at 2:00 p.m. ET and will be moderated by Chris Ciufu, group editorial director, OpenSystems Publishing.

The webcast will include an overview by Tom Cox, executive director of the RapidIO Trade Association as well as presentations from RapidIO Trade Association members Freescale Semiconductor, IDT, Mercury Computer Systems, and Tundra Semiconductor Corporation.

"This webcast presents a unique opportunity for the design engineering community to learn about the RapidIO eco-system's commitment to interoperability, interworking, next-generation product development, and multi-vendor system level application deployment, all critical steps in facilitating design using RapidIO technology," noted Tom Cox, executive director, RapidIO Trade Association.



For information on the webcast visit www.opensystems-publishing.com or www.RapidIO.org, or register at: <http://w.on24.com/r.htm?e=25912&s=1&k=2925A2B5C449695FAA291AC7A61F81B9&partnerref=rapid>

RapidIO Radio September Program To Feature IDT Addressing RapidIO Technology in the Wireless Infrastructure

In a relatively short period of time, our reliance on wireless communications devices has grown exponentially: from the commonplace wireless Bluetooth headsets seen on virtually every other person walking down the street today to the ability to carry personalized communication, information, and entertainment with us in our cars, our computers, our pockets and even as jewelry.

This escalating demand has put incredible strains and demands on service providers to create and rapidly deploy an exceedingly high-performance, reliable wireless infrastructure. To meet this need, manufacturers need flexibility and scalability, as well as the ability to create modular designs – traits that RapidIO technology deliver, and that make this standard a key component of wireless infrastructure designs. On September 25th, Bill Beane, Senior Product Manager, FCM Division, at Integrated Device Technology and an active member of the RapidIO Trade Association will discuss *The Benefits Of Serial RapidIO In Achieving Flexibility And Scalability In Wireless Infrastructure*.

The final 2006 podcast is scheduled for December 2006 and will feature QNX discussing software considerations. The 2007 schedule will be available in Q4. To download any of the RapidIO Radio presentations, visit www.RapidIO.org and click on the RapidIO Radio button at the top of the screen.



Industry Insights

Interworking: Solidifying The Complementary Roles Of PCI Express, RapidIO And Ethernet In Next-Generation Systems

by Ann Thryft, Senior Editor, RTC Magazine and COTS Journal

The interconnect landscape looks pretty crowded right now, with several I/O standards emerging that appear to compete for chip-to-chip and board-to-board interfaces. The three main interconnect choices are Ethernet, PCI Express (PCIe) and RapidIO. Although these share certain similarities and compete in some areas, each is finding a place in the larger landscape of system architecture.

Many switched fabrics, such as PCIe and the serial version of RapidIO, Serial RapidIO, share common electrical and signaling characteristics, making it easy for designers and integrators to mix fabric-specific solutions based on off-the-shelf silicon with fabric-agnostic products that use FPGAs. Although most switched fabric interconnects share a common physical layer, their capabilities and the topologies they support differ considerably.

Since this is the era of everything-over-IP, and therefore everything-over-Ethernet, Ethernet and its variations will continue to be deployed in a widening range of uses, especially for network connectivity and IP-based data traffic. Switched Gigabit Ethernet is becoming the preferred interconnect for high-speed, high-bandwidth IP networks connecting subsystems and chassis.

Subsystem- and board-level products are, of course, dependent on their chip ecosystems. While Ethernet functionality has been included in systems and chips for some time, PCIe and RapidIO are rapidly joining it. PCIe is now found widely as an emerging standard for board-to-peripheral interconnects. In addition, PCIe is being included as a native processor interface on embedded CPUs and is appearing on an increasing number of merchant communications chips. The result is a rise in its use for chip-chip interconnections.

RapidIO is being used to interconnect DSPs and PowerPCs, especially in telecom. This is only logical, since the standard was originally developed for communications and networking applications, as well as signal processing. Serial RapidIO interfaces will appear on more CPUs this year.

Serial RapidIO, like the Advanced Switching Interconnect (ASI) evolution of PCIe, was initially designed as a peer-to-peer fabric, and both support several topologies beyond the hierarchical tree structure of PCIe. Both Serial RapidIO and ASI will probably be used to provide chassis-wide and multi-chassis switched fabrics that interconnect system nodes. In particular, Serial RapidIO will likely be found performing data movement in high-performance, next-generation military signal processing systems because of its more efficient packet structure, flexible network topologies and higher bandwidth (10 Gbytes/s total).

Technical Insights

Designing Next-Generation Wireless Systems: an FPGA-centric approach using XtremeDSP and Serial RapidIO solutions

By Narinder Lall, Senior Manager, DSP Product and Solutions Marketing, Xilinx, Inc.,
narinder.lall@xilinx.com

The demands of next-generation wireless infrastructures require system designers to address not only processing bottlenecks, but connectivity bottlenecks. Today's domain optimized FPGAs provide the ideal mix of high-performance DSP to handle the most demanding chip-rate and radio algorithms and serial MGTs, addressing high-speed connectivity and interoperability challenges.

Tomorrow's wireless infrastructure equipment designers will face an increase in algorithmic complexity and data rate brought on by the convergence of data, video, and voice. Solutions based on discrete devices such as microprocessors, DSPs, and transceivers provide tremendous headaches related to interoperability and latency, and can quickly drive up both cost and power per channel.

An FPGA-centric approach that combines high-performance DSP capability and Serial RapidIO will help alleviate some of these system performance bottlenecks and provide an integrated solution that better meets economic and energy constraints. In addition, an FPGA-centric approach provides designers with the flexibility to recover from mistakes and make hardware changes even after system deployment, thereby reducing overall design risk.

The DSP Industry Embraces Serial RapidIO

Figure 1 shows that in the late 1990s, GSM systems that provided voice communications only supported terminal data rates below 10 kbps. In contrast, W-CDMA systems, which started rolling out in 2002, needed to support voice, data, and video, and hence used 2 Mbps data rates. Future systems such as W-CDMA (HSDPA) and CDMA2000 (1xEV-DO and DV) will use data rates greater than 2 Mbps.

Designers have implemented

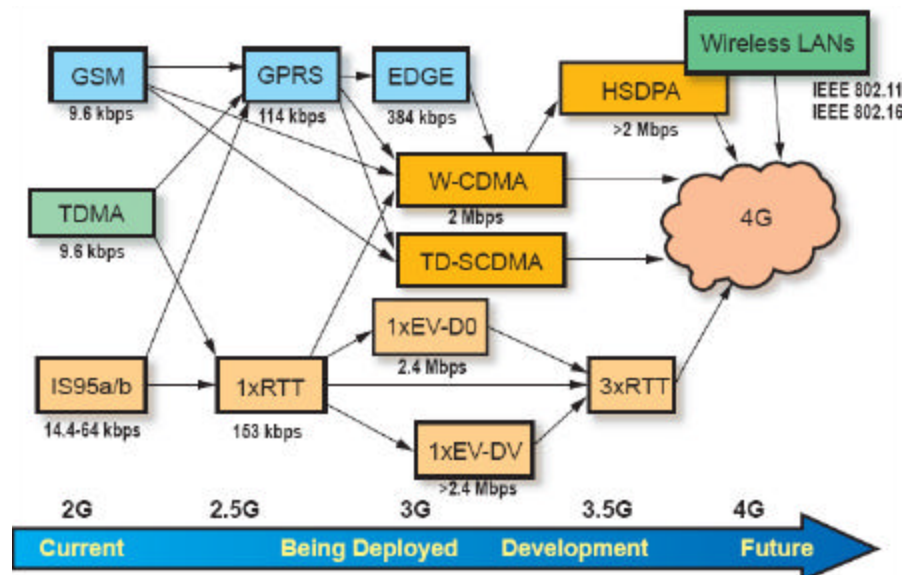


Figure 1

ASICs – and more increasingly FPGAs – in wireless systems to handle digital radio (modulation/demodulation, DDC/DUC) and high-chip-rate processing. FPGAs exploit parallel processing techniques through hard-wired embedded multipliers and provide the flexibility to make algorithmic changes even after system deployment, saving millions in maintenance or field upgrade costs.

Second, the need to transport such high information packets presents new connectivity challenges. Traditional buses are fast running out of bandwidth. Wide parallel buses are becoming too complicated to design and increasingly difficult to scale. As serial I/O technology begins to mature, wireless infrastructure equipment designers are looking towards system interconnect architectures based on MGTs to handle their transport problems. This gives rise to potential chip-to-chip and board-to-board interoperability headaches for system designers.

What is encouraging is that leading DSP IC suppliers that supply chip-rate and symbol-rate processing solutions (such as Texas Instruments™, Motorola™, and Xilinx®) are at the forefront of the Serial RapidIO revolution and are keen to address connectivity and interoperability challenges in next-generation wireless infrastructure systems.

Figure 2: High performance domain-optimized FPGAs incorporate embedded high-



Figure 2

performance DSP capability, Serial RapidIO connectivity, and control functions through embedded PowerPC™ 405 processors. As chip-rate processors, FPGAs provide an ideal complement to DSP processors, which have traditionally been used for lower sample- and symbol-rate processing.

Serial RapidIO Benefits Using FPGAs

FPGAs provide a number of benefits to wireless infrastructure equipment designers:

- ⌘ High-performance throughput provides the necessary bandwidth to cope with next-generation data transport needs.
- ⌘ Lower complexity software and an ability to complete peer-to-peer transactions simplifies systems. It also provides a well-defined mechanism for congestion control.
- ⌘ A flexible, low-risk solution offers scalable bandwidth options for future demands and fast time to market.



- ✍ With many DSP and other system IC (microprocessor, ASIC) vendors committing to Serial RapidIO, designers will have architectural flexibility.
- ✍ Lower system cost through the use of a small silicon footprint and high bandwidth efficiency.

One such implementation could use an FPGA solely as a central switch between chip and symbol-rate devices.

Conclusion

The availability of Serial RapidIO-based ASICs, FPGAs, and DSPs provides a number of options for implementing wireless infrastructure systems. FPGAs provide system designers with another means to further enhance system throughput, lower cost-per-channel, and retain the flexibility of an FPGA-centric solution. For more information visit www.xilinx.com.



Design Tips

Serial RapidIO Switching in Wireless Infrastructure

By Keri Zingle, Product Marketing Engineer, PMC-Sierra

Wireless infrastructure vendors are pursuing implementations using AdvancedTCA® and MicroTCA™ architectures with Serial RapidIO interconnect. Within these systems, Serial RapidIO can be implemented for card-to-card connections, or for intra-card local interconnect. Each of these interconnect applications requires a switch with specific features to meet the needs of the application.

For Wireless Basestations, vendors using standard hardware are choosing MicroTCA, because it provides a more compact, lower cost solution than the AdvancedTCA form factor. Basestations implement MicroTCA in a dual-star configuration, offering 1+1 protection for the switch fabric, i.e. working and protecting MicroTCA Carrier Hubs (MCH). Each basestation supports multiple DSP Advanced Mezzanine cards (AMC), which are treated as a pool of resources to be shared by all antennae.

On MCH cards, the Serial RapidIO switch needs to be a high density, high capacity device that can be implemented in a single stage, providing power, space, and cost savings over multi-chip solutions. For full connectivity, the switch should have 16 ports that can scale to address the bandwidth growth occurring between baseband processors and radio interfaces. Scaling from low link rate to high link rate, and from 1x to 4x links per port, provides expanded capacity as additional carriers and sectors get added. For traffic distribution, latency through the switch must be minimized, as I/Q samples are periodic and highly time-sensitive. Further, the switch should be configurable to allow higher priority to the ports connected to the Radio interface cards (biased arbitration).

For local interconnect on baseband processing cards, the Serial RapidIO switch should support 1x links for connection to DSPs, and 4x links for connection to the MCH. DSP connections are short and have no intervening connectors, while MCH connections go over a backplane across 2 connectors. Therefore, electrical characteristics of the switch ports must support short-range and long-range interconnect environments.

For higher capacity wireless applications such as 3G Radio Network Controllers (RNC) or Media Gateways, systems integrators are implementing AdvancedTCA in a dual-star configuration with 1+1 protection for the switch fabric. The AdvancedTCA carrier cards in these systems may house up to 4 AMC modules, or use the entire carrier area for a pool of DSPs. Each processor card will be connected to the working and protect core switch fabric.

In these high-capacity computing applications, fast protection cut-over is critical to ensure a robust system in the event of fabric failure. The Serial RapidIO switch should implement a hardware based cut-over trigger, such as device pins or a single register write, for



immediate response to failure. Switches located at the AdvancedTCA carrier cards should treat the ports connected to the Working and Protect core fabric cards as a Port Pair. The routing tables should be configured only to the level of specifying the Port Pair. A control function can direct traffic to either port within the pair based on the operational status of the two fabric cards.

On the carrier cards, DSPs can be connected in a single stage, with switches located on the AdvancedTCA carrier card. The switch requires high density, low capacity ports (x1) to DSPs with high capacity ports (x4) to the central switch or other switches. Alternatively, a two level switch can be implemented, in which switches are located on the AMCs and on the carrier cards.

PMC Sierra's PM6352 RSE 160 switch implements key features that address card-to-card and local interconnect applications. Connection between the core fabric to every card in an AdvancedTCA or a MicroTCA chassis can be implemented in a single device. The integrated high-performance SERDES ensures signal integrity across the backplane. For high availability, the device supports hardware-based APS cut-over, with biased arbitration for traffic selection, and low latency. For local interconnect the RSE 160 scales to support 1.25G, 2.5G or 3.125G over one or four links, depending on application requirements. Wireless infrastructure vendors can utilize the RSE 160 switch for end-to-end Serial RapidIO connectivity. For more information, visit www.pmc-sierra.com.



Events

Meet up with RapidIO Trade Association members and see their products first hand at a range of industry events. Dates subject to change, check <http://www.rapidio.org/events/list/> for current details and information.

Global RapidIO Design Summit – North America	<p>Engineering managers, system architects, and embedded product developers are invited to attend the RapidIO Trade Association’s Boston Global RapidIO Design Summit, which will provide valuable information on RapidIO technology and products and include working demonstrations in the technology lab. Sessions, application papers and design tips will be presented by RapidIO Trade Association members including Fabric Embedded Tools Corporation (FET), Freescale Semiconductor, FuturePlus Systems, Integrated Device Technology (IDT), Jennic, Mercury Computer Systems, Texas Instruments, Tundra Semiconductor Corporation, and Xilinx.</p> <p>www.RapidIO.org/events/design_summits_2006/designsummit2006/</p>	<p>August 17, 2006 9:00 a.m. - 5:30 p.m. Woburn Plaza Hotel Boston, MA</p>
The State of RapidIO E-Cast	<p>The RapidIO Trade Association and OpenSystems Publishing (OSP) are teaming up to sponsor a webcast covering the latest RapidIO technology advancements and specification updates. The event, “RapidIO System Architecture: What Designers Need to Know,” will be moderated by Chris Ciufu, group editorial director, OpenSystems Publishing.</p> <p>http://w.on24.com/r.htm?e=25912&s=1&k=2925A2B5C449695FAA291AC7A61F81B9&partnerref=rapid</p>	<p>August 24, 2006 2:00 p.m. ET</p>
RapidIO Radio	<p>Bill Beane, Senior Product Manager, FCM Division, at IDT and an active member of the RapidIO Trade Association will discuss <i>The Benefits Of Serial RapidIO In Achieving Flexibility And Scalability In Wireless Infrastructure</i>.</p>	<p>Download available September 25, 2006</p>
AdvancedTCA Summit	<p>The RapidIO Trade Association will be hosting a number of technical and application sessions focusing on the RapidIO technology and standard.</p>	<p>Oct. 17-19, 2006 Santa Clara, CA</p>
Global RapidIO Design Summit -	<p>Engineering managers, system architects, and embedded product developers are invited to attend the RapidIO Trade Association’s Japan Global RapidIO Design Summit, which will provide valuable information on RapidIO technology and products and include</p>	<p>October 20, 2006 Tokyo,</p>



Japan	working demonstrations in the technology lab.	Japan
Global RapidIO Design Summit - China	Engineering managers, system architects, and embedded product developers are invited to attend the RapidIO Trade Association's China Global RapidIO Design Summit, which will provide valuable information on RapidIO technology and products and include working demonstrations in the technology lab.	October 24, 2006 Shenzhen, China
Global RapidIO Design Summit - China	Engineering managers, system architects, and embedded product developers are invited to attend the RapidIO Trade Association's China Global RapidIO Design Summit, which will provide valuable information on RapidIO technology and products and include working demonstrations in the technology lab.	October 25, 2006 Shanghai, China
Global RapidIO Design Summit - India	Engineering managers, system architects, and embedded product developers are invited to attend the RapidIO Trade Association's India Global RapidIO Design Summit, which will provide valuable information on RapidIO technology and products and include working demonstrations in the technology lab.	November 29, 2006 Bangalore, India



In the News

During the past three months, The RapidIO Trade Association, its members and their products continue to be sought after news in the industry.

- ✍ **Freescale Semiconductor** (NYSE:FSL, FSL.B) has introduced its third-generation multicore DSP based on next-generation SC3400 StarCore technology. The new MSC8144 DSP is engineered to deliver leading-edge performance, reduce system costs and significantly increase channel densities for next-generation wireline and wireless infrastructure applications providing voice, video and data services.
- ✍ **IDT** (Integrated Device Technology, Inc.; NASDAQ: IDTI) announced the industry's only off-the-shelf pre-processing switch (PPS) for digital signal processor (DSP) clusters. Optimized for wireless baseband processing applications and utilizing the Serial RapidIO interconnect, the IDT PPS is an advanced semiconductor solution integrating an innovative suite of byte- and packet-level manipulation capabilities designed to offload DSPs of specific bandwidth-intensive tasks. This offload can accelerate each DSP within a cluster by up to 20 percent, thereby enabling the processors to focus on other compute-intensive functions related to meeting the requirements of next-generation wireless infrastructure design. The PPS is the first in a series of forthcoming IDT products designed to offer a complete data-acceleration solution for DSPs and other key components in wireless baseband processing applications, allowing customers to create scalable, flexible, and cost-effective solutions.
- ✍ **Mercury Computer Systems, Inc.** (NASDAQ: MRCY - News) announced a family of starter kits for commercial off-the-shelf (COTS) developers, at the Military Embedded Electronics and Computing Conference (MEECC) in Long Beach, CA. Mercury also announced details and availability of the first starter kit in the series, which is based on its performance-leading PowerStream 6100 series RapidIO VXS multicomputer.
- ✍ **Mercury Computer Systems, Inc.** (NASDAQ: MRCY) announced the availability of its reconfigurable computing variant of the Mercury PowerStream® 7000 multicomputer. The PowerStream 7000 FCN (FPGA Compute Node) can incorporate up to 69 Xilinx® seven-million-gate field-programmable gate arrays (FPGAs) connected by a RapidIO switch fabric, enabling twice the processing performance in the same system footprint.
- ✍ **Tundra Semiconductor Corporation** (TSX: TUN) announced the Tundra Tsi574 Serial RapidIO Switch, a high-performance switch with patent-pending technology that delivers the performance, power and configurability, designers of embedded designs need to build reliable, high-performance RapidIO-based systems for a wide



range of applications such as wireless base stations, media gateways, video infrastructure and DSP-intensive image processing.

- ✍ **Tundra Semiconductor Corporation** (TSX: TUN) announced the Tundra Tsi576 Serial RapidIO Switch, a low price per port, small footprint device with optimal port width configurations for both the local and backplane interconnect. The Tsi576 expands the Company's high-performance RapidIO(R) switch portfolio targeted for a wide variety of DSP-based applications such as wireless base stations, media gateways, video infrastructure and image processing.

Following are some of the many places where the RapidIO Trade Association made headlines between May and July 2006.

- ✍ *ATCA Newsletter*
- ✍ *CommsDesign.com*
- ✍ *CompactPCI and AdvancedTCA Systems*
- ✍ *Connector Specifier*
- ✍ *DigiTimes Bits + chips*
- ✍ *Design & Reuse*
- ✍ *DMN Newswire*
- ✍ *DSP-FPGA.com*
- ✍ *EDACafe.com*
- ✍ *EDA Geek*
- ✍ *EDN*
- ✍ *EE Times*
- ✍ *EE Times Asia*
- ✍ *EE Times / EE Times Product Center*
- ✍ *Industrial Embedded Systems*
- ✍ *IT News Online*
- ✍ *Light Reading*
- ✍ *Linley Group*
- ✍ *LinuxDevices.com*
- ✍ *MILCOTS Digest*
- ✍ *Military Embedded Systems*
- ✍ *Netscape Celebrity*
- ✍ *Netstumbler.com*
- ✍ *Nikkei Electronics Asia Online*
- ✍ *Ottawa Business Journal*
- ✍ *Physorg.com*
- ✍ *RF Design*
- ✍ *Telecom Asia*



- ✂ *EFY Times*
- ✂ *Eg3*
- ✂ *Electronic Design*
- ✂ *Electronicstalk*
- ✂ *Electronicsweekly*
- ✂ *Electropages*
- ✂ *Embedded Computing Design*
- ✂ *E Product Alert*
- ✂ *Ferret.com*
- ✂ *RTC Magazine*
- ✂ *Test & Measurement World*
- ✂ *TMCnet*
- ✂ *The 451 Group*
- ✂ *VoIP Magazine*
- ✂ *VMEbus Systems*
- ✂ *Wikipedia, the free encyclopedia*
- ✂ *Yahoo! News*

Visit these links to read a sampling of the articles that include RapidIO technology, its members and RapidIO-based products:

- ✂ *ATCA Newsletter: Freescale expands AdvancedTCA ecosystem with modular reference designs*
http://www.atcanewsletter.com/English/Collaterals/Vendor_Press_Releases/2005/20050622_Freescale_Ecosystem.pdf
- ✂ *CommsDesign.com: Serial IO toolkit simplifies debug of Virtex-4 FX RocketIO transceivers*
<http://www.commsdesign.com/showArticle.jhtml?articleID=185300002>
- ✂ *CompactPCI and AdvancedTCA Systems: RapidIO System Architecture: What Designers Need to Know*
<http://www.compactpci-systems.com/eletter/>
- ✂ *DigiTimes Bits + chips: NEC chooses Xilinx Virtex-4 FPGAs for 40 Gbps WDM optical communications systems*
http://www.digitimes.com/bits_chips/a20060508PR205.html
- ✂ *Design and Reuse: Tundra Expands Industry-Leading Portfolio of Serial RapidIO(R) Switches*
<http://www.us.design-reuse.com/news/news13452.html>
- ✂ *DSP-FPGA.com: IDT Enhances Efficiency of Next-Generation Wireless Infrastructures with Industry's Only Pre-Processing Switch*



- <http://www.dsp-fpga.com/news/db/?3137>

⌘ DSP-FPGA.com: New High-Performance Freescale DSP Capitalizes on Full Potential of Serial RapidIO Technology Debugging Capabilities

<http://www.dsp-fpga.com/news/db/?2827>
- ⌘ EDACafe.com: Tundra Expands Serial RapidIO(R) Switch Portfolio With Launch of New 12 Port, Low Power, Small Footprint Switch

http://www10.edacafe.com/nbc/articles/view_article.php?section=ICNews&articleid=290905
- ⌘ EDN: Quad-core DSP packs performance and features

<http://www.edn.com/article/CA6335292.html?ref=nbsa&text=DSP&text=DSP&text=rapidio>
- ⌘ EE Times Asia: Serial RapidIO switch targets DSP-intensive apps

http://www.eetasia.com/ART_8800420444_499491_147376e3200606_no.HTM
- ⌘ EE Times / EE Product Center: DSP uses RapidIO technology to enable triple-play communications applications

http://www.eeproductcenter.com/dsp/brief/showArticle.jhtml;jsessionid=J01JEUXWB4TC0Q_SNDBECKHSCJUMEKJVN?articleID=187203470
- ⌘ EFY Times: TI, Tata Elxsi Deliver 802.16e Demonstration System

<http://www.efytimes.com/fullnews.asp?edid=12300>
- ⌘ Electronic Design: One Smart Serial RapidIO Switch

<http://www.elecdesign.com/Articles/Index.cfm?AD=1&ArticleID=12972>
- ⌘ Electronicstalk: Podcast explains the benefits of RapidIO

<http://www.electronicstalk.com/news/rai/rai108.html>
- ⌘ Electronicstalk: Lab gathers support for compliance testing

<http://www.electronicstalk.com/news/rai/rai107.html>
- ⌘ Electronicsweekly: IDT pre-processor offloads DSP tasks

<http://www.electronicweekly.com/Articles/2006/07/18/39262/IDT+pre-processor+offloads+DSP+tasks.htm>
- ⌘ Electropages: IDT - First off-the-shelf pre-processing switch for DSP clusters

<http://www.electropages.com/viewArticle.aspx?intArticle=7249>
- ⌘ Embedded Computing Design: Chips & cores: FPGA

<http://www.embedded-computing.com/products/search/fm/id/?17750>



- ⌘ *Embedded Computing Design: Enea's OSEck DSP RTOS First to Support Freescale's New MSC8144 Multicore DSP*
<http://www.embedded-computing.com/news/db/?2813>
- ⌘ *Embedded Computing Design: Freescale and Wind River Unite to Deliver Optimized Networking and Communications Platforms*
<http://www.embedded-computing.com/news/db/?2846>
- ⌘ *Embedded Computing Design: RapidIO Trade Association Announces Fall 2006 Global Design Summits in North America, Japan, South Korea, China, and India*
<http://www.embedded-computing.com/news/db/?3122>
- ⌘ *E Product Alert: Defining an Open Standard Fabric*
<http://www.eecatalog.com/interconnect/article.php?article=6>
- ⌘ *E Product Alert: Fault-Tolerant Systems and RapidIO®*
<http://www.eecatalog.com/interconnect/article.php?article=7>
- ⌘ *ferret.com: FuturePlus Systems selects Agilent Technologies' logic analyzers*
<http://www.ferret.com.au/articles/da/0c0404da.asp>
- ⌘ *IT News Online: Freescale Develops PowerQUICC III Multicore Processor Architecture*
<http://www.itnewsonline.com/showstory.php?storyid=4796&scatid=3&contid=3>
- ⌘ *Light Reading: Tundra Announces Tsi574*
http://www.lightreading.com/document.asp?doc_id=95906
- ⌘ *LinuxDevices.com: ATCA platform runs CGL, open source management suite*
<http://www.linuxdevices.com/news/NS9382332259.html>
- ⌘ *MILCOTS Digest: RapidIO Trade Association Launches Radio Podcasts*
<http://www.milcotsdigest.com/Articles/2006/April/News/Default.htm>
- ⌘ *Netscape Celebrity: RapidIO(R) Radio Episode 2: Interoperability, A Crucial Factor In System Design*
<http://channels.netscape.com/celebrity/story.jsp?idq=/ff/story/5722/20060626/1042276475.htm>
- ⌘ *Nikkei Electronics Asia: Serial RapidIO Switches*
<http://neasia.nikkeibp.com/neasia/004558>
- ⌘ *RF Design: Freescale introduces industry's highest-performance fully programmable digital signal processor*



http://rfdesign.com/next_generation_wireless/news/freescale_introduces_processor/index.html

✉ *RTC Magazine: System Scalability with Switched Fabrics in CompactPCI*

<http://www.rtcmagazine.com/home/article.php?id=100652>

✉ *Test & Measurement World: FuturePlus Systems' SERIAL RAPIDIO probe works with Agilent analyzers*

<http://www.reed-electronics.com/tmworld/article/CA6317111.html>

✉ *TMCnet: RapidIO Radio Episode 2: Interoperability, A Crucial Factor In System Design*

<http://www.tmcnet.com/usubmit/2006/06/26/1695475.htm>

✉ *VoIP Magazine: Freescale Introduces Industry's Highest-Performance Fully Programmable Digital Signal Processor; New Quad-Core MSC8144 Based on Next-Generation StarCore Technology Delivers Performance Equivalent to a 4GHz Single-Core DSP*

<http://www.voip-magazine.com/content/view/3201/20060516005111/>

✉ *VMEBus Systems: Mercury Computer Systems Announces Availability of RapidIO-Based VXS Starter Kit; First in COTS Starter Kit Series*

<http://www.vmebus-systems.com/news/db/?2828>

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