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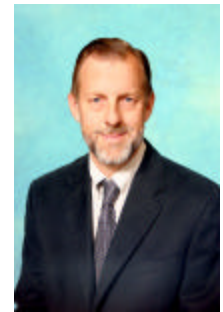
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Next Generation Spec Release: Supporting Current RapidIO Deployment with a Roadmap to Higher Performance and Greater Functionality

By Tom Cox, Executive Director
RapidIO Trade Association



The importance of a roadmap takes on different context for engineers and technology managers depending on many factors which are unique to each individual's current challenges. For many having a roadmap to the next faster, smaller and more efficient product, service or technology provides insurance that their solution is future-proof. For many others who live on the very brink of technology's leading edge, it represents a solution they believe they need now or sooner.

The RapidIO standard has a strong history of serving today's requirements with widely available, affordable technology while at the same time mapping out and delivering on a roadmap to meet the needs of tomorrow. RapidIO technology was created with a layered spec which forms the foundation for 'future-proofing'. The three layers of the specification can be modified, updated and added to individually while maintaining backwards compatibility and with interoperability in mind.

The RapidIO physical layer is one of the most apparent examples of feature and function additions to the RapidIO technology suite. The first physical layer defined by the RapidIO standard in 2000 was the Parallel LVDS I/O. This provided the lowest latency and the highest data throughput, critical for very high performance computing, and enabled RapidIO technology to develop a strong presence in military applications. The second physical layer defined for RapidIO technology was the Serial 1Gbps, 2.5Gbps and 3.125Gbps XAUI interface.

With 1x and 4x pairs defined, this serial RapidIO interface today is found on dozens of devices ranging from DSPs, CPUs and switches to endpoints, ASICs and FPGAs. This serial interconnect generation will service the bulk of the requirements for a wide range of market applications for the next 10 years or more.

The future of the RapidIO physical layer story does not end there, however. The RapidIO Technical Working Group has been defining the next generation physical layer spec over the past two years. The next added option for high-speed fabric interconnects in RapidIO is 5Gbps and 6.25 Gbps with added options to channel widths. To be released later this year, the specification is currently in ballot for final open industry standards ratification. For many, 5 Gbps and 6.25 Gbps are beyond the current needs of the applications they support, but they represent an important option for the future for interconnection between individual fabric switch chips. Of course for a few facing the most demanding application requirements, this high performance is a requirement not matched by any other available solution. With the full backward compatibility with any flavor of RapidIO protocol and the ability to mix and match speeds and widths to the problem at hand, more speed and added options for granularity are appealing.

The new RapidIO technology spec also adds important logical layer functions. These logical layer and transport layer functions enhance the RapidIO interconnects' data management capability. Driven by key system OEMs' the new RapidIO spec adds significant data plane enhancements to offer carrier grade data fabric performance. These features include new data streaming packet format, addition of virtual channels (VCs) to serial physical layer, new endpoint flow control arbitration, and virtual output queue (VoQ).

Deployment of RapidIO technology continues to focus on high bandwidth with low overhead, a complete set of transaction types including memory mapped I/O, message passing, globally shared memory, and streaming data. The new functions of the spec will enable carrier grade data fabric performance with deterministic latency with end-to-end data management in a higher level of quality of service. Whether you are looking for the next step forward in technology now or in the future, the RapidIO standard delivers!

RapidIO Radio Episode 3: RapidIO Delivers the Flexibility and Scalability Needed to Achieve Modular Wireless Infrastructure Design

Episode 4, "Software Considerations Around RapidIO Designs," due out in December.

Episode 3 of RapidIO® Radio from the RapidIO Trade Association is immediately available for download at www.RapidIO.org and www.iTunes.com. The third in a series, "RapidIO Delivers the Flexibility and Scalability Needed to Achieve Modular Wireless Infrastructure Design," explores some of the critical design issues facing the wireless infrastructure design community, and ways RapidIO technology has solved these challenges while delivering superior performance. The program is hosted by Tom Cox, the executive director of the RapidIO Trade Association, and features Bill Beane, senior product manager, FCM Division for IDT.

The final 2006 podcast "Software Considerations Around RapidIO Designs," explores some of the critical software issues facing the wireless infrastructure design community, and ways RapidIO technology has solved these challenges while delivering superior performance. is scheduled for December. The program, with Jim Parisien, president of Fabric Embedded Tools, will provide basic information that listeners can take back to the lab and put to use at the board and system level. In doing so, Jim Parisien, president of Fabric Embedded Tools, will examine some of the features built-in to the RapidIO standard that facilitate debugging of both software and hardware systems.

In 2007, RapidIO Radio will return with an expanded schedule beginning in January with Greg Shippen, system architect at Freescale Technology who will talk with Tom Cox about the benefits of RapidIO vs. Ethernet. <http://www.rapidio.org/wp/>

"RapidIO: The Embedded System Interconnect," the Definitive Guide to RapidIO Technology, Now Available in Simplified Chinese

Based on demand from the global engineering community, "RapidIO: The Embedded System Interconnect" is now available in simplified Chinese. The book, a recognized expert source, provides a detailed description of RapidIO applications in several types of systems, and is the first comprehensive reference on the RapidIO interconnect technology. The book is available through the RapidIO Trade Association and on Amazon.com. "RapidIO: The Embedded System Interconnect" is an essential tool for professionals involved in the development of large-scale, high-performance, high availability embedded networking, communications and related equipment. With contributions from industry leaders, this book also serves as

an excellent reference for common RapidIO packet and symbol formats, register file definitions, and system software application programming interfaces. For more information contact the RapidIO Trade Association, www.rapidio.org/about/contact/.

System Interconnect Fabrics: Ethernet vs. RapidIO, a Comprehensive and Definitive White Paper Focusing on Practical Considerations for Design, Now Available through the RapidIO Trade Association

A comprehensive white paper, System Interconnect Fabrics: Ethernet vs. RapidIO, by RapidIO Trade Association Steering Committee Member Greg Shippen, has been published on the RapidIO web site, www.RapidIODIRECTLINK.org. This authoritative work begins with a general overview of what System Interconnects need to look like, moves through thorough technical discussions of Ethernet and RapidIO technologies, leading to an in-depth comparison of the two technologies as well as practical considerations for their use.

Beginning in Q1 2007, the white paper will serve as the foundation for industry-wide review and discussion through articles, podcasts, and webinars, and at industry events. Greg Shippen, the author, is a system architect for Freescale Semiconductor's Digital Systems Division, NCSG. For more information on events around this paper, visit the RapidIO web site, www.RapidIO.org, often.

Industry Insights

Interworking: Solidifying the Complementary Roles of PCI Express, RapidIO and Ethernet in Next Generation Systems

By Ernie Bergstrom, VP Research & Chief Analyst, Crystal Cube Consulting LLC

Crystal Cube Consulting (CCC) in its review of Next Generation Networks (NGN) and their development have monitored and tracked the major high-speed switch fabric architectures including RapidIO, Advanced Switching Interconnect (ASI), which recently became lifeless for the foreseeable future, InfiniBand, HyperTransport and Fibre Channel since 2003. It has been clear to us the direction that RapidIO has taken since the beginning, which was to set their sights on providing a transparent high-speed bus architecture aimed at delivering multiple connectivity and interoperability utilizing switching architecture as the control point for I/O connectivity. To that end RapidIO has taken a very obvious commanding lead in the high-speed bus architecture for embedded system. So with the announcement that Intel's ASI was being abandoned by a majority of its supporters, RapidIO was truly elated and well prepared to embrace their business model to address support for PCI Express and Ethernet.

Since its first inception, RapidIO has developed an eco-system of components and suppliers which provides the technology for the complementary roles of PCI Express along with RapidIO and Ethernet. Serial RapidIO switches decrease overall system cost, power and latency while providing distributed processing locally for DSPs and CPU's. The key advantages utilizing Switched Serial RapidIO architectures include low and deterministic latency between processing elements with lower power and low cost interconnect. Multicast support provided by RapidIO is another critical area for reducing latency in such applications as wireless base-band and video devices.

Currently CCC, with the research we have continued to do in the switch fabric architecture arena, see a definite heating-up of switch fabric architecture activity, if you will, in the communications sector between PCI Express and the competing Serial RapidIO interconnect supported by Freescale Semiconductor, Texas Instruments, Tundra and others. Unlike ASI, RapidIO is gaining traction as an interface for PowerPCs and digital signal processors, especially as a way to link the farms of DSPs found in wireless base stations and video.

The RapidIO Trade Association has created strong ties with tier-one OEMs. Last fall, representatives from Lucent Technologies, Ericsson and storage company EMC were elected as association officers. Several companies appear to be at the point where they plan to make commitments with RapidIO and are not likely to use ASI. Even if some companies were electing to revisit ASI in the future, as a possible high-speed switch fabric architecture, it appears to CCC that it would be some time before ASI could have a viable plan in place for high-speed architecture solutions for embedded systems.

There are those out there, however, that believe the rising adoption of PCI Express could have some market impact on RapidIO. PCI Express has such a large eco-system that some companies are recommending that people put native PCI Express interfaces on their communications chips. The situation seems to be that companies, in being prudent, need to consider how many DSPs will add PCI Express in the future. If that were to become quite common it could have an impact on RapidIO's continued strong growth, but that remains to be seen. Nevertheless with ASI stepping aside, and remembering ASI was to solve the shortcomings of a PCI Express solution in a fabric architecture, certainly puts RapidIO in a very strong position in the market place.

One of the RapidIO member companies, Applied Micro Circuits Corp (AMCC) sells a PowerPC 440SPE processor that sports three Express interfaces and is geared for storage systems. It will announce its first CPUs with serial RapidIO before the end of the year, and also plans more devices using PCI Express. They are doing PCI Express, Ethernet and Serial RapidIO, and are the three interfaces that will be the processors of choice going forward, according to Sam Fuller, vice president of marketing at AMCC. Freescale ships a half dozen PowerPCs and one DSP using Serial RapidIO. Texas Instruments has two high-end DSPs using Serial RapidIO.

The flexibility that RapidIO offers with their serial switch fabric allows them to produce different products from the same hardware and software architecture, as well as the scalability to produce different classes of products with the same hardware and

software architecture. Additionally, RapidIO can and will provide connectivity in their switch fabric architecture solutions to include PCI Express and Ethernet where the solution makes sense or is in the client's best interest. Flexibility is the name of the game for RapidIO's success moving forward.

Technical Insights

PCIe and RapidIO Work Together

By Charles Frazier, Mercury Computer Systems, Inc.

www.mc.com

System designers are faced with many challenging problems to solve and therefore, need a variety of technologies to best architect their solutions. In the world of interconnects, the prolific PCI Express connectivity technology works well for small systems and connecting I/O devices, while RapidIO technology is designed for low latency, high performance, and highly deterministic operation. Combining these two technologies can enhance system design and make solutions significantly better than if only one of the technologies is used.

PCI Express at the I/O

PCI Express was designed for the desktop computer market and thus its architecture works well in a system that incorporates one master and a few slave I/O devices. The proliferation of PCI Express has created many chipsets that connect to standard I/O technologies, such as Ethernet, SATA, Fibre Channel, and many others, making PCI Express ideally suited to extend to standard interconnects. But scaling of PCI Express systems to large processor systems that work on real-time events is limited due to its inherent non-real-time design.

RapidIO as the system fabric

In many applications, processing requirements have grown beyond what individual processors can deliver. This performance mismatch has created the need for a multi-peer fabric that enables the distribution of processing among many processing elements. These requirements for system connectivity and features such as flow control, data streaming, multicast, and high reliability were the driving force behind the creation of RapidIO.

The Complete System Solution

Many embedded systems have used PCI Express based components because of the large number of standard I/O interfaces and processors that it supports. A problem occurs, however, if the computational task requires scaling the system to many processors. PCI Express is not well suited to address this problem. Many embedded systems require robust I/O connectivity and very high processing rates. The

combination of PCI Express enabled processors, which have robust I/O connectivity, and RapidIO fabric can provide a solution to the challenges of these demanding embedded applications.

RapidIO technology is extremely flexible and is designed to meet the stringent requirements of redundancy imposed by such industries as communications, which require topologies like dual star, mesh, and other complex designs. On the other end of the spectrum, RapidIO topologies can be configured in a daisy-chain fashion to reduce costs and meet the needs of pipelined processing systems. Figure 1 shows a typical small PCIe processor-based system using RapidIO as the interconnect technology. The PCIe-to-RapidIO bridge performs many functions, such as address translation, memory protection, multithreaded DMA, and a host of other functions. Bridges from such

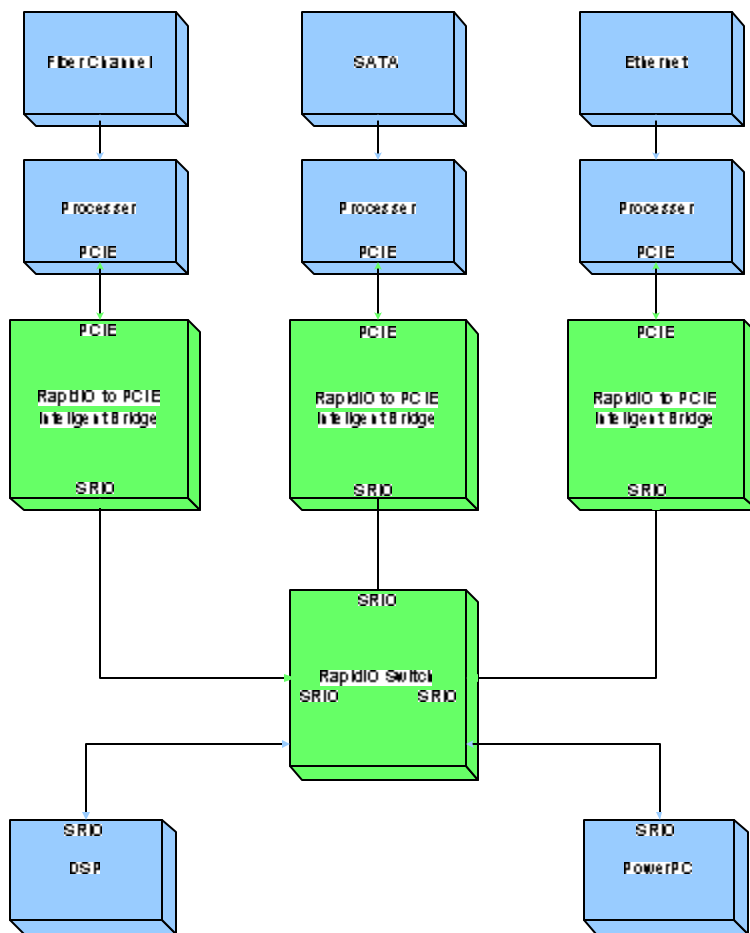


Figure 1: Typical mixed serial RapidIO and PCI Express system

vendors as Mercury Computer Systems offload a significant amount of data-moving tasks from the processor and operate at line rate.

Many embedded systems require synchronization among the various processing elements. This requirement has been designed into the RapidIO specification in a variety of ways.

- ✍ Atomic operations – Enable synchronization
- ✍ Response-based transactions – When packets are received at a destination, a response packet can be sent back acknowledging receipt
- ✍ Message passing (hardware-based) – Enables data to be shared among various processors, where management of ownership is provided
- ✍ Multicast TOD event – Enables time synchronization in the <math><1 \mu\text{s}</math> range among processors in a system using in-band communications

Complementary technologies

RapidIO was designed and architected from the ground up as a multiprocessor fabric to meet the demanding needs of the multiprocessor environment. PCI Express was designed to enable I/O expansion from a single processor and has excellent bandwidth, low cost, I/O connectivity, and a software infrastructure to enable turnkey I/O connectivity. The complementary technologies of a serial RapidIO based fabric and PCI Express I/O connectivity enable designers to create systems that can take advantage of the strengths of these two interconnects for better overall performance.

The 10G Serial Buffer: Bringing Advanced Memory Solutions to the RapidIO Ecosystem

By Michael Olsen, Integrated Device Technology

www.IDT.com

The Problem: Increasing the Ability to Buffer Serial Packets in High-Bandwidth RapidIO Systems

Typically, high-throughput environments — such as wireless base stations and other digital signal processor (DSP)-intensive applications – consume large amounts of system resources, including high-density memory.

For example, today's wireless base stations need to see the same set of data multiple times to decode different sets of information. Specifically, in 3G systems the same hardware module (DSP or chip rate processing ASIC) needs to access 10ms of sample frame data to do random access channel (RACH) decoding first, and data channel (DCH) second, with this same data being accessed by all of the DSPs in the cluster. This sample-compare memory problem generally requires the consumption of costly system resources to achieve the requisite speed and limits the capacity of the base station system to support value-added services at a competitive price point.

One approach is to break the large samples into fragments for nested calculation, but this consumes extra processing cycles and reduces overall throughput. Another is to dramatically enlarge one local memory on a board for use as a buffer that feeds the other local memories. This complicates memory management and only serves as a band-aid that mitigates the bottleneck problem somewhat, but does not solve it. And yet a third approach is to store the data in FPGA/DSP combinations — a custom design with high design cost/risk. Clearly, a new approach is mission-critical to the success of providing cost-effective, high-performance systems.

The Solution: Bringing a 10G Serial Buffer into the RapidIO Ecosystem

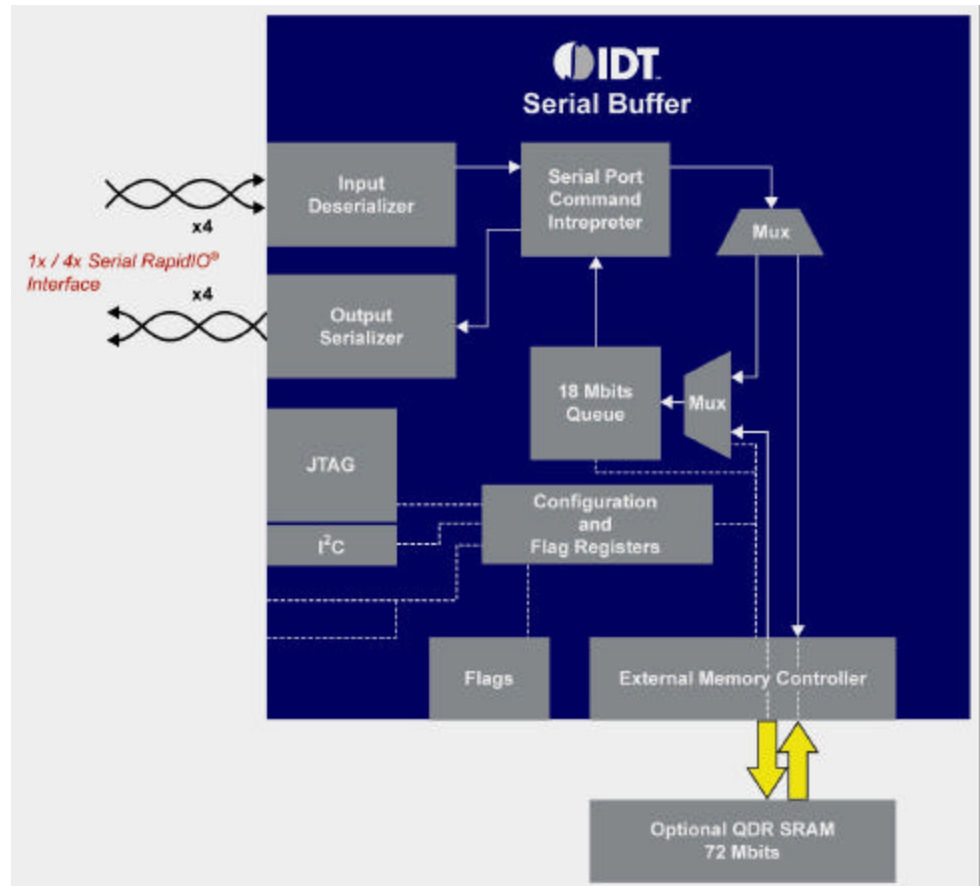
Enabling true 10 Gbps data transfer rates for DSP-intensive applications, with comparatively low I/O count and BOM, the 10G serial buffer is the first and only Serial

RapidIO®-based memory available today. Depending upon the specific alternative approach used for comparison, the 10G serial buffer can:

- ✍ Dramatically improve performance by eliminating local memory bottlenecks, or
- ✍ Reduce silicon area by eliminating or reducing the need for local memory entirely, or
- ✍ Significantly simplify design by eliminating complex memory management schemes

Able to connect to any serial RapidIO switch or end-point, the 10G serial buffer has 18 Mbits of internal memory, plus connection to 72 Mbits of external QDR SRAM—another industry first. This sum total of 90 Mbits enables a DSP to compare consecutive data samples in one calculation, thus eliminating the time-consuming nested calculations required by capacity-limited local memories.

Moreover, the 10G serial buffer contains intelligent monitoring and control circuitry that automatically identifies and compensates for dropped data packets to maintain data synchronicity — a vital function for high-performance systems. This product can also operate as a master, recognizing when and where data must be sent, and initiating data transfers with no additional assistance



from the DSPs or other RapidIO end-points in the system.

Note that while the example above described a base station application, the 10G Serial Buffer will also meet the needs of other applications requiring large buffers. For instance: medical imaging (CAT scans, MRIs — anywhere that larger files are being transferred), high-speed communications applications (large lines that need to be

buffered), and any DSP-cluster applications (such as radar, data-acquisition and sampling).

Events

Meet up with RapidIO Trade Association members and see their products first hand at a range of industry events. Dates subject to change, check <http://www.rapidio.org/events/list/> for current details and information.

<i>RapidIO Design Summit - India</i>	<i>Engineering managers, system architects, and embedded product developers are invited to attend the RapidIO Trade Association's India Global Design Summit, which will provide valuable information on RapidIO technology and products and include working demonstrations in the technology lab.</i>	<i>Nov 29, 2006 The Leela Palace Hotel Bangalore, India</i>
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In the News

During the past three months, The RapidIO Trade Association, its members and their products continue to be sought after news in the industry.

✍ **Fabric Embedded Tools Corporation** (FET) announced the availability of its version 2.1 release of RapidFET™ which leverages host capable Serial RapidIO endpoints such as Texas Instruments Incorporated (TI) digital signal processors (DSPs). RapidFET is a network management and diagnostic tool proven to work well with TI's TMS320C6455 and TMS320TCI6482 DSPs to configure systems quickly, isolate problems and manage system traffic. The enumeration, auto discovery and other network management features enabled by the combination of RapidFET software on TI's communication infrastructure focused DSPs, enable homogenous systems with DSP taking on more of system host and management functionality.
www.rapidio.org/news/pr/view?item_key=c94e9111f29c44bf8720721a469f63501db80c33

✍ Broadband access equipment manufacturers now can integrate control and data path functions onto a single semiconductor device with the introduction of an advanced PowerQUICC III processor family from **Freescale Semiconductor** (NYSE: FSL, FSL.B). Compatible with previous generation PowerQUICC offerings, Freescale's MPC8568E and MPC8567E processors offer a Gigahertz CPU core, flexible QUICC Engine technology and high speed system interfaces

for multi-protocol interworking.

www.rapidio.org/news/pr/view?item_key=4e19dff246c2f14e639b8feaae2f49c81c537e2f

- ✍ **IDT** (Integrated Device Technology, Inc.) (NASDAQ: IDTI), a vital semiconductor solutions provider, announced that its industry-leading pre-processing switch (PPS) secured first place in the EE Times and eeProductCenter 3.2 Ultimate Products survey. Nominated in the logic/programmable logic and interface products category, the IDT 70K2000 PPS is the industry's only off-the-shelf pre-processing switch (PPS) supporting digital signal processor (DSP) clusters in wireless base station applications. More specifically, the product is designed to enable wireless cell phone users to receive high value-added services, such as mobile video, by way of modular wireless infrastructures designed to achieve higher throughput at a lower price point.

www.rapidio.org/news/pr/view?item_key=fda1d6eb99ba3a89951aa004715af4674b589c8d

- ✍ **Lattice Semiconductor** (NASDAQ: LSCC) announced that Mercury Computer, a computing solutions provider to government, defense, energy, medical and telecommunications providers, has ported its high-performance Serial RapidIO® Intellectual Property (IP) product line, consisting of x1 and x4 endpoint IP cores, to the LatticeSC family of 90nm (nanometer) Extreme Performance FPGAs. In addition, Mercury has joined Lattice's ispLeverCORE Connections IP partner program. Working together, Mercury and Lattice will develop and deliver complete system solutions for mutual customers requiring high-performance Serial RapidIO connectivity supported by Lattice's FPGA product families.

www.rapidio.org/news/pr/view?item_key=430f5dec45499df6c32a37c44df3ede8342caf83

- ✍ **Mercury Computer Systems, Inc.** (NASDAQ: MRCY - News) announced its Serial RapidIO®-to-PCIe Bridge IP (intellectual property) Core – the first intelligent bridge of its kind in the industry. The Serial RapidIO-to-PCIe intelligent bridge features complete protocol translation, an optimized dual-channel multi-threaded DMA engine, and a pipelined PCI Express-to-RapidIO mapping table to address high-throughput streaming applications as both consumer and producer. It also provides a variety of system service features including mailbox message queuing, PCIe MSI/MSI-X interrupt controller, RapidIO-to-PCIe Atomic transaction encapsulation, access protection, real-time event counters, and error management.

www.rapidio.org/news/pr/view?item_key=0ec87067cbc8b8da9bef8ba1d68a9e3d61d281ae

- ✍ **Texas Instruments Incorporated** (TI), along with members of the TI DSP Third Party Network, delivered in-depth technical presentations on several signal processing topics to attendees of the Global Signal Processing Conference (GSPx) Silicon Valley and the GSPx Multi-Core Applications Conference, held from

October 30 - November 2 at the Santa Clara Convention Center. These presentations are designed to introduce and educate designers on innovative products and ground-breaking signal processing technologies. In addition to system level programming tips for TI's DaVinci(TM) technology, TI sessions will give designers a deep dive into the Serial RapidIO (sRIO) and Message Queue functionality of the TMS320C6455 digital signal processor (DSP).

www.rapidio.org/news/pr/view?item_key=78f122ba5f84887dca5bda624ca9d049e93efcdd

✍ **Tundra Semiconductor Corporation** (TSX: TUN), the leader in System Interconnect, announced that Emerson Network Power's (NYSE: EMR) new Embedded Computing business, formerly Artesyn Communication Products, has implemented Tundra's industry-leading Tsi568A Serial RapidIO Switch into the Fat Pipe switch module in its new 12-slot MicroTCA development system, and is working with Tundra on a series of additional Serial RapidIO designs.
www.rapidio.org/news/pr/view?item_key=68349c734ee16e9dd85842397d1f78c90dcf6092

✍ **Tundra Semiconductor Corporation** (TSX:TUN), the leader in System Interconnect, announced availability of the Tundra Tsi578 Serial RapidIO Development Platform (SRDP). The addition of this design support tool, using the Tsi578 Serial RapidIO Switch, offers customers flexibility and the overall benefit of reducing both their design risk and time-to-market.
www.rapidio.org/news/pr/view?item_key=6db8bd23df6c8413a62e9fc94eee93641ea88368

In the Spotlight:

During the last few months, The RapidIO® Trade Association and standard continue to be sought after news in the industry. Following are some of the many places where the RapidIO Trade Association is making headlines and many of these outlets ran multiple stories between August 2006 and October 2006.

✍ *Advanced Imaging Pro*

✍ *Analog and DSP*

✍ *ArriveNet*

✍ *Bolsamania*

✍ *Byte & Switch*

✍ *Chip Design*

✍ *CommsDesign.com*

✍ *Control Engineering*

✍ *COTS Journal*

✍ *Daily Business News*

✍ *Desktop Engineering*

✍ *Design & Reuse*

✍ *DMN Newswire*

✍ *DSP-FPGA.com*

✍ *ECN Asia*

✍ *EE Times Asia*

✍ *EE Times India*

- ✍ *EE Times / EE Times Product Center*
- ✍ *Eg3*
- ✍ *Electronic Design*
- ✍ *Electronic Products*
- ✍ *Embedded.com*
- ✍ *Embedded Computing Design*
- ✍ *Embedded Control Europe*
- ✍ *HPCwire*
- ✍ *KCAU-TV*
- ✍ *KOTA Territory News*
- ✍ *Light Reading*
- ✍ *LinuxDevices.com*
- ✍ *LinuxElectrons*
- ✍ *Managing Automation*
- ✍ *Military & Aerospace Electronics*
- ✍ *MILCOTS Digest*
- ✍ *Military Embedded Systems*
- ✍ *Monitor Today*
- ✍ *Planet Analog*
- ✍ *RTC Magazine*
- ✍ *Sys-con India*
- ✍ *Tickertech.com*
- ✍ *Wireless Design & Development*
- ✍ *Wireless Net DesignLine*
- ✍ *Yahoo! Finance*
- ✍ *Yahoo! News*

Visit these links to read a few of the articles including RapidIO technology, member companies, and products:

- ✍ *Advanced Imaging Pro: Mercury Computer Systems Announces the First Available Serial RapidIO-to-PCIe Bridge IP Core,*
<http://www.advancedimagingpro.com/article/article.jsp?id=3340&siteSection=3>
- ✍ *Analog and DSP: Freescale Launches Next Generation PowerQuicc II,*
<http://www.analoganddsp.com/results.asp?entryid=8846>
- ✍ *ArriveNet: MVA Launches Communications Ecosystem Conference,*
<http://press.arrivenet.com/technology/article.php/844229.html>
- ✍ *ArriveNet: Customers Accelerate their Time-to-Market with new Tundra Serial RapidIO Development Platform,*
<http://press.arrivenet.com/industry/article.php/860602.html>
- ✍ *Byte & Switch: RapidIO Reaffirms Commitment,*
http://www.byteandswitch.com/document.asp?doc_id=104084
- ✍ *Chip Design: Serial RapidIO-to-PCIe Bridge IP Core,*
<http://www.chipdesignmag.com/display.php?articleId=631&issueId=0>
- ✍ *CommsDesign.com: Freescale integrates Quicc engine with e500 CPU core,*
<http://www.commsdesign.com/news/showArticle.jhtml?articleID=193200077>
- ✍ *Control Engineering: Tundra Semiconductor, Atmel to provide system interconnect products,*

- <http://www.manufacturing.net/ctl/article/CA6359244.htm?spacedesc=industryUpdates>
- ✍ *COTS Journal*: AMC/ATCA Boards Target SRIO and GbE Backplanes,
<http://www.cotsjournalonline.com/home/article.php?id=100561&pg=4>
 - ✍ *Desktop Engineering*: Mercury Announces PowerStream 6600,
<http://www.deskeng.com/Departments/Products/Products%3A-October-2006-200609191287.html>
 - ✍ *DMN Newswire*: Customers Accelerate their Time-to-Market with new Tundra Serial RapidIO Development Platform,
<http://www.dmnnewswire.com/articles/viewarticle.jsp?id=73070>
 - ✍ *DSP-FPGA.com*: Achieving modular wireless infrastructure design: A compelling look at benefits supporting connectivity amongst DSPs, FPGAs, or ASICs, <http://www.dsp-fpga.com/eletter/>
 - ✍ *ECN Asia*: FET Leverages Serial RapidIO-Based Tool,
<http://www.ecniamag.com/article.asp?id=10447>
 - ✍ *EE Times Asia*: Serial RapidIO-to-PCIe Bridge IP core reduces system development time,
http://www.eetasia.com/ART_8800436957_590626_76fd64f6200610_no.HTM
 - ✍ *EE Times Asia*: RapidIO design summits set in Tokyo, Bangalore,
http://www.eetasia.com/ART_8800434567_590626_814d7fc7200609_no.HTM
 - ✍ *EE Times Asia*: Upgraded RapidFET complements TI DSPs in network management,
http://www.eetasia.com/ART_8800434316_499495_3c0e8a7c200609_no.HTM
 - ✍ *EE Times Asia*: Multi-computer suits military C4ISR multimode missions,
http://www.eetasia.com/ART_8800432354_499495_77d5ce79200609_no.HTM
 - ✍ *EE Times / EE Product Center*: Tool lets DSPs configure Serial RapidIO systems,
<http://www.eeproductcenter.com/dsp/brief/showArticle.jhtml?articleID=192700350>
 - ✍ *EE Times / EE Product Center*: RapidIO(R) Trade Association Announces Details of 2006 Asia-Pacific Global RapidIO Design Summits,
<http://www.eeproductcenter.com/showPressRelease.jhtml;jsessionid=SWOFRO3TIXHOOQSNDLPCKH0CJUNN2JVN?articleID=X528078>
 - ✍ *EE Times / EE Product Center*: Market Leaders Reaffirm Commitment and Long-term Support for the Open RapidIO(R) Interconnect Architecture Standard,
<http://www.eeproductcenter.com/showPressRelease.jhtml;jsessionid=SWOFRO3TIXHOOQSNDLPCKH0CJUNN2JVN?articleID=X528437>

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