

Serial RapidIO Gen 2 (2.0 & 2.1)  
Specification Update  
October 2009



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# Revision 2.0 Review



- Public Release in March 2008
- Provides higher performance while maintaining low protocol overhead
- Backwards compatible with 1.3 specification
- Two major areas of concentration
  - New higher performance physical layer
    - 5.0 and 6.25Gbaud rates added with DFE
    - 2x, 8x, and 16x link width options added
    - Data scrambling and new control symbol functionality added
  - Significant Data Plane enhancements
    - Virtual Channels (VCs) added to Serial Physical Layer
    - Virtual Output Queue (VoQ) specification added
    - Data Streaming Packet Format (Type 9 packet)
    - New Endpoint flow control arbitration and traffic management

# Revision 2.1 Enhancements



- Approval in August 2009
- Public release in September 2009
- Goal was to further enhance the specification by enabling additional high speed link implementations and broaden the market applications
- Enhancements include:
  - Mode to facilitate short 5Gbaud links without DFE and with the IDLE1 control symbol
  - Increased robustness of the IDLE2 operation
- These changes will encourage adoption of the higher performance RapidIO specification in a wider range of applications where the conditions demand performance with an aggressive TTM requirement
- The consolidated 2.0/2.1 specification will officially be referred to as Serial RapidIO Gen 2

# Key RapidIO1.3 to Gen2 Feature Comparison



Part	Change Description	1.3 to 2.0	2.0 Spec Section	2.0 to 2.1	2.1 Spec Section
6	Added support for 5 Gbaud and 6.25 Gbaud lane rates	X	Part 6		
6	Added support for 2x, 8x, and 16x ports	X	Part 6 4.6		
6	Support for Virtual Channels 1-8 in physical layer	X	Part 6 2.2		
12	Added Virtual Output Queueing Backpressure specification	X	Part 12		
10	Note that support for Type 9 is optional.	X	Part 10, 1.1		
10	Added 'Extended Header' support to Type 9.	X	Part 10, 4.3		
6	Idle2 Sequence, Long Control Symbols and Data Scrambling Required for 6.25 Gbaud lane rates only.			X	Part 6 3.1

Backup Information  
Full Comparison Table  
RapidIO 1.3 to Gen2 Specifications



# Revision 1.3 vs. 2.0 vs. 2.1 Detail - 1



Item	Part	Change Description	1.3 to 2.0	2.0 Spec Section	2.0 to 2.1	2.1 Spec Section
1	1	Maintenance read responses with status of ERROR may optionally include data in the response.	X	Part 1, 4.1.10		
2	1	Type 13 packets with status of Error may be either TTYPE 0 or 8, but must not have data.	X	Part 1, 4.2.3		
3	1	Addition of 'Multiport' bit in Processing Element Features CAR.			X	Part 6 6.4.1
4	1	Switch Port Information CAR required if 'Multiport' bit is '1', regardless of the state of bit 3 of the Processing Element Features CAR.			X	Part 6 6.4.1
5	2	Message passing interface annex was specifically labelled as 'informative'	X	Part 2 Annex A		
6	3	Devices must support 'promiscuous mode' for packet reception.	X	Part 3 2.3		
7	3	Recommended that devices always process maintenance read requests, regardless of device ID values.	X	Part 3 2.3		
8	3	Changed requirement for presence of Standard Route Configuration Destination ID Select CSR from bit 23 to bit 22 of the Processing Element Features CAR.	X	Part 3 3.5.4		
9	6	<b>Added support for 2x, 8x, and 16x ports</b>	X	Part 6 4.6		
10	6	<b>Added support for 5 Gbaud and 6.25 Gbaud lane rates</b>	X	Part 6		

# Revision 1.3 vs. 2.0 vs. 2.1 Detail - 2



Item	Part	Change Description	1.3 to 2.0	2.0 Spec Section	2.0 to 2.1	2.1 Spec Section
11	6	Idle2 Sequence, Long Control Symbols and Data Scrambling Required for 5 Gbaud and 6.25 Gbaud lane rates.	X	Part 6 3.1		
12	6	<b>Idle2 Sequence, Long Control Symbols and Data Scrambling Required for 6.25 Gbaud lane rates only.</b>			X	Part 6 3.1
13	6	<b>Support for Virtual Channels 1-8 in physical layer</b>	X	Part 6 2.2		
14	6	Virtual Channel Bandwidth Allocation Register Block	X	Part 6 6.7		
15	6	6 bit ackIDs when IDLE2 Sequence/Long control symbols are used on a link. 5 bit ackIDs when IDLE1 Sequence/Long Control Symbols are used on a link.	X	Part 6 2.2		
16	6	Added VC bit to packet physical layer header	X	Part 6 2.2		
17	6	The ackID field in Packet-Not-Accepted control symbols is undefined	X	Part 6 3.4.3		
18	6	Added 'No Resources' and 'Loss of Descrambler Sync' to the Packet-Not-Accepted cause field.	X	Part 6 3.4.3		
19	6	Added VC Status control symbol type	X	Part 6 3.4.5		
20	6	Added Enter/Exit Loopback control symbol commands to Link Request Control Symbol.	X	Part 6, 3.5.5.1, 3.5.5.2		

# Revision 1.3 vs. 2.0 vs. 2.1 Detail - 3



Item	Part	Change Description	1.3 to 2.0	2.0 Spec Section	2.0 to 2.1	2.1 Spec Section
21	6	Remove Enter/Exit Loopback Control Symbol commands from Link Request Control Symbol.	X	Part 6, 3.5.5		
22	6	Long Control Symbol uses CRC-13.	X	Part 6 3.6.3		
23	6	Optional Baud Rate Discovery feature enabled in the PMA layer.	X	Part 6 4.12.3		
24	6	Support for Adaptive equalization function in the PMA layer.	X	Part 6 4.12.3		
25	6	Definition of Comma	X	Part 6 4.5.6		
26	6	Definition of valid and invalid code-groups			X	Part 6 4.5.6
27	6	Definition of illegal code groups.			X	Part 6 4.5.7.8
28	6	Added use of the Mark ( /M/,  M  ) code group to the IDLE2 sequence	X	Part 6 4.5.7.7		
29	6	All Nx ports must support 1x operation	X	Part 6 4.6		
30	6	All Nx ports must support 'fail down' to redundant 1x operation.	X	Part 6 4.6		

# Revision 1.3 vs. 2.0 vs. 2.1 Detail - 4



Item	Part	Change Description	1.3 to 2.0	2.0 Spec Section	2.0 to 2.1	2.1 Spec Section
31	6	Clarification of IDLE1 sequence definition, always starts with clock compensation sequence, and may be terminated any time after the first 4 characters/columns.	X	Part 6 4.5.9		
32	6	Clarification of IDLE2 sequence			X	Part 6 4.7.4.1.1
33	6	Completely reorganized IDLE2 command fields within the IDLE2 frame.			X	Part 6 4.7.4.1.3
34	6	Requirement for a 250 msec timeout for action on an IDLE2 command.			X	4.7.4.1.4
35	6	1x/2x Mode Detect state machine definition			X	Part 6 4.12.4.4
36	6	All link initialization state machines have changed (ongoing)	X	Part 6 4.12	X	Part 6 4.12
37	6	Increased discovery timer interval to 28 +/- 4 msec			X	Part 6 4.12.4.1.3
38	6	Defined striping rules for ports which are wider than 4x.	X	Part 6 4.10		
39	6	Added concept of reliable traffic (RT) and continuous traffic (CT), linked to VC1-8 operation.	X	Part 6 5.1		
40	6	Rules for scheduling among VCs have been defined.	X	Part 6 5.11		

# Revision 1.3 vs. 2.0 vs. 2.1 Detail - 5



Item	Part	Change Description	1.3 to 2.0	2.0 Spec Section	2.0 to 2.1	2.1 Spec Section
41	6	Specifacaton of column padding for 8x & 16x ports	X	Part 6 4.10		
42	6	Detection of a column padding error for 8x & 16x ports (padding characters do not descramble to D0.0 characters)	X	Part 6 5.13.2.1		
43	6	Definition of IDLE2 sequence errors	X	Part 6 5.13.2.2.2		
44	6	Clarification that packets cancelled with a Link-Request control symbol when IDLE2 is active shall have no errors reported if the only errors detected were the presence of /M/ special characters in the packet, and possibly the detection of a packet of excessive length.			X	Part 6, 5.13.2.4
45	6	Clarification that nothing may be transmitted between the data scrambling SYNC sequence and the link-request control symbol.			X	Part 6, 4.8.2
46	6	Reception of a Packet-Retry control symbol when operating in Multi-VC mode.	X	Part 6 5.13.2.3.1		
47	6	Additional error scenarios: Control symbol's start delimiter does not occur in lane number X, where X modulo 4 = 0, and detection of a long control symbol with unequal start and end delimiters	X	Part 6 5.13.2.3.2		

# Revision 1.3 vs. 2.0 vs. 2.1 Detail - 6



Item	Part	Change Description	1.3 to 2.0	2.0 Spec Section	2.0 to 2.1	2.1 Spec Section
48	6	Input error-stopped recovery process extended to cover operation in multi-VC mode, and with reliable/continuous traffic flows	X	Part 6 5.13.2.6		
49	6	Addition of 'Multiport' bit in Processing Element Features CAR.			X	Part 6 6.4.1
50	6	Switch Port Information CAR required if 'Multiport' bit is '1', regardless of the state of bit 3 of the Processing Element Features CAR.			X	Part 6 6.4.1
51	6	Retransmit suppression on error' function removed - Processing element features CAR bit 25 is now implementation specific	X	Part 6 6.4.1		
52	6	Increased field widths in Port n Local ackID CSR to accommodate 6 bit ackIDs	X	Part 6 6.7		
53	6	Port n Error and Status added: Bit 0: IDLE2 support Bit 1: IDLE2 enable Bit 2: Current Idle sequence active Bit 28: Port Unavailable indication	X	Part 6 6.6.8		
54	6	Port n Error and Status added: Bit 4: TX/RX Flow control active			X	Part 6 6.6.8
55	6	Port n Control CSR 16-17: Extended Port-Width override 18-19: Extended Port-Width support 20-27: Changed to implementation defined from 'retransmission suppression mask'	X	Part 6 6.6.9		

# Revision 1.3 vs. 2.0 vs. 2.1 Detail - 7



Item	Part	Change Description	1.3 to 2.0	2.0 Spec Section	2.0 to 2.1	2.1 Spec Section
56	6	Added Port n Control 2 CSR	X	Part 6 6.6.10		
57	6	Added 'Data Scrambling Disable' and 'Inactive Lanes Enable' to Port n Control 2 CSR.			X	Part 6 6.6.10
58	6	Clarification that 'Data Scrambling Disable' does not affect scrambling of D0.0 characters within the IDLE2 random data field			X	Part 6 4.8.1
59	6	Added support for 'Inactive Lanes Enable'			X	Part 6 4.12
60	6	Added LP-Serial Lane Extended Features Block			X	Part 6 6.7
61	6	Added VC Extended Features Block	X	Part 6 6.7		
62	6	Removed packing of VC Extended Features Block registers			X	Part 6 6.8.1
63	6	Signal names changed to allow for up to 16 lanes.	X	Part 6 7		
64	6	Electrical specification clarified for 1.25, 2.5 and 3.125 Gbaud lanes	X	Part 6 Chapters 8, 9		
65	6	Specification of 5.0 and 6.25 Gbaud lanes, short and long reach transmitter.	X	Part 6 Chapter 10		
66	6	Made the input/output common mode voltage identical for short, medium and long reach transmitters/receivers.			X	Part 6, Table 10-2 and 10-6

# Revision 1.3 vs. 2.0 vs. 2.1 Detail - 8



Item	Part	Change Description	1.3 to 2.0	2.0 Spec Section	2.0 to 2.1	2.1 Spec Section
67	6	Added requirement that skew between signals of a differential pair at the transmitter pins must not exceed 15 ps.			X	Part 6 10.4.2.1, 10.4.2.1.5
68	6	BERR rate lowered to 10 <sup>-15</sup> for 5 & 6.25 Gbaud links	X	Part 6, Chapter 8		
69	6	Clarification of how link reinitialization affects link error status, link initialized state and port initialized state.			X	Part 6 5.5.3.1
70	7	Add requirement for promiscuous mode (process packets with any source/destination ID) on exit from reset.	X	Part 7 3.2.1.1		
71	8	Detection of a packet with a destination ID that is undefined is allowed for all processing elements (including switches), not just endpoints.	X	Part 8, 2.3.2.2		
72	8	Requirements for data capture on error are added, including capture of packet/control symbol data, and capture of K/D 10B character indications in the implementation specific field of the Port n Attributes Capture CSR			X	Part 8 1.2.1, 2.3.2
73	8	Modification of physical error rate control and status operation for VC's.			X	Part 8, 1.2.3, 2.3.2
74	8	Clarified which Error Management registers/fields are read only and which are read/write.			X	Part 8, 2.3.2

# Revision 1.3 vs. 2.0 vs. 2.1 Detail - 9



Item	Part	Change Description	1.3 to 2.0	2.0 Spec Section	2.0 to 2.1	2.1 Spec Section
75	8	Clarification of delineation error (29), received illegal or invalid character (15), and received data character in IDLE1 sequence (16) for Port n Error Detect/Enable CSRs			X	Part 8, 2.3.2.10, 2.3.2.11
76	8	Bit 15 and bit 16 are now optional in the Port n Error Detect/Enable CSRs			X	Part 8, 2.3.2.10, 2.3.2.11
77	8	Extension of Port n Attributes Capture CSR to include specification of long control symbol capture			X	2.3.2.12
78	9	Improved explanation of how Flow Control fits in the RapidIO network.	X	Part 9, 1.2		
79	9	Addition of an optional Flow Arbitration protocol with support for Fixed/Static Resource Allocation, and Dynamic Resource Allocation.	X	Part 9, 2.2		
80	10	<b>Note that support for Type 9 is optional.</b>	X	Part 10, 1.1		
81	10	<b>Added 'Extended Header' support to Type 9.</b>	X	Part 10, 4.3		
82	10	Definition of 'Physical Channel ID', and clarification of 'RapidIO flow'.	X	Part 10, 1.5		
83	10	Destinations are permitted to define their use of Virtual Stream IDs to pre-associate certain kinds of traffic with certain end processes.	X	Part 10, 3.2.2		

# Revision 1.3 vs. 2.0 vs. 2.1 Detail - 10



Item	Part	Change Description	1.3 to 2.0	2.0 Spec Section	2.0 to 2.1	2.1 Spec Section
84	10	Added Data Streaming Traffic Management bit 12 to Source/Destination Operations CARs	X	Part 10, 5.4.1, 5.4.2		
85	10	Added bits 0-7 of the Data Streaming Logical Layer Control CSR to control what Flow Arbitration protocol aspects are in use.	X	Part 10, 5.5.1		
86	11	Addition of data streaming error detection to Logical/Transport error detection registers.			X	Part 11 5.4
87	12	<b>Added Virtual Output Queueing Backpressure specification</b>	X	Part 12		

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